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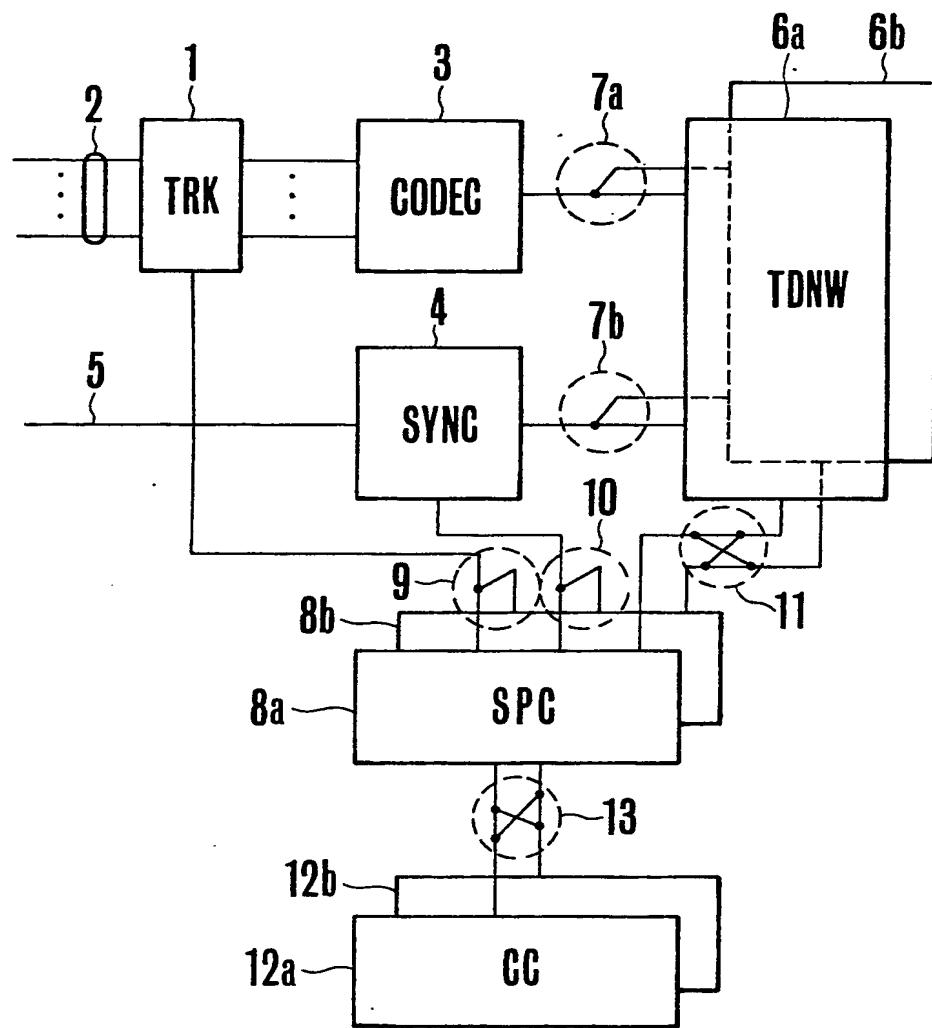
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(54) Time division telephone switching systems

(57) The telephone switching system comprises a plurality of speech path units, a juncture switch unit for interconnecting the speech path units, a central processing unit for controlling the speech path units and the juncture switch unit. Each speech path unit comprises a time switch which shifts a signal which is time-division-multiplexed from time slots of a plurality of incoming highways to other time slots on a plurality of outgoing highways, a digital trunk circuit for processing a register signal received by the time slot and other control signals, and speech path control equipment which receives and distributes a control signal between the time division switch, the digital trunk circuit and the central processing unit. The juncture switch unit is constructed to change the connections between the speech path units by switching time slots in groups treating a plurality of connections as a single cell. This simplifies the holding store of the space stage and facilitates extension and switching to a reserve speech path unit in the event of a fault.

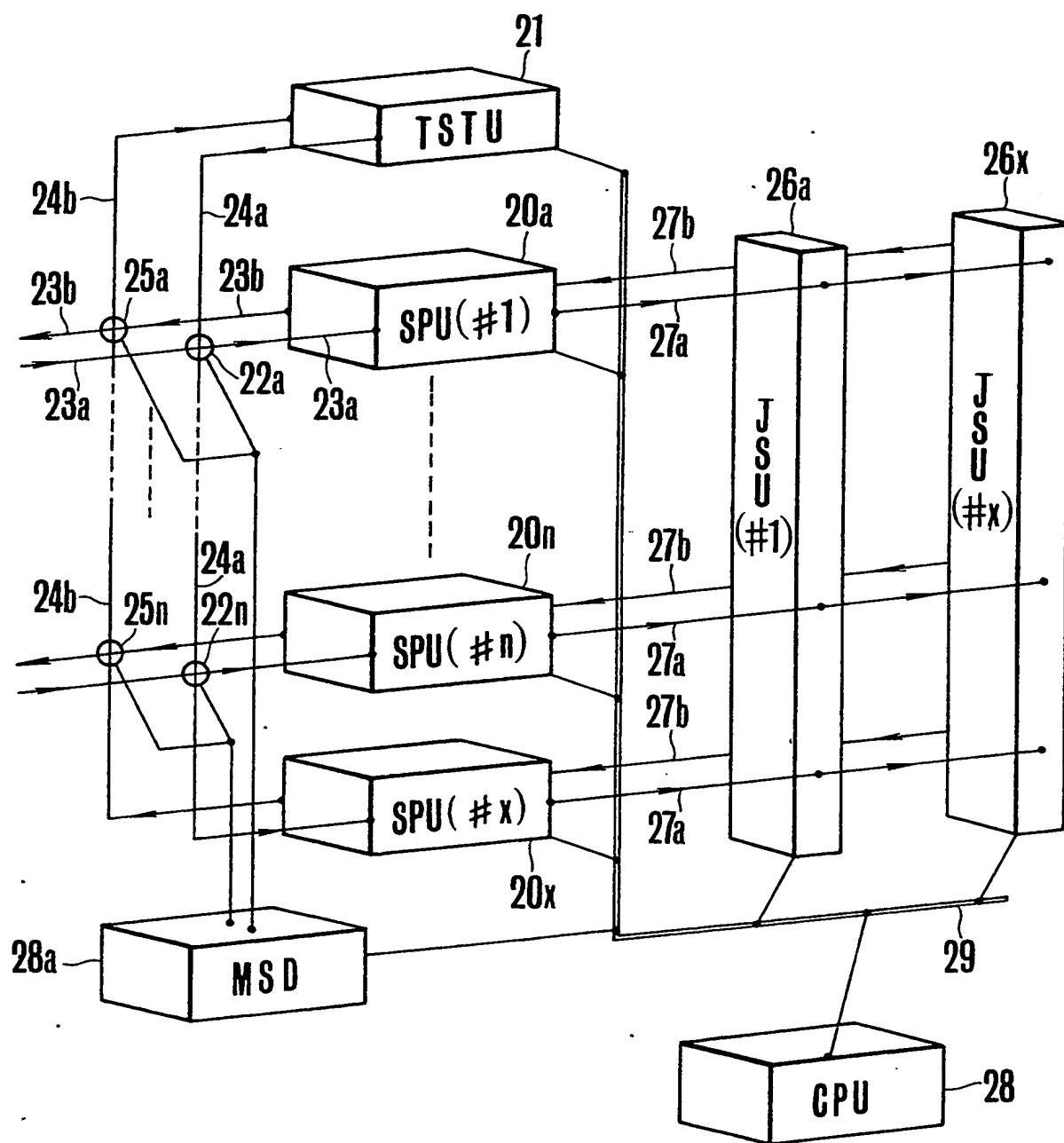
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FIG. 1
PRIOR ART

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FIG.2



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FIG.3

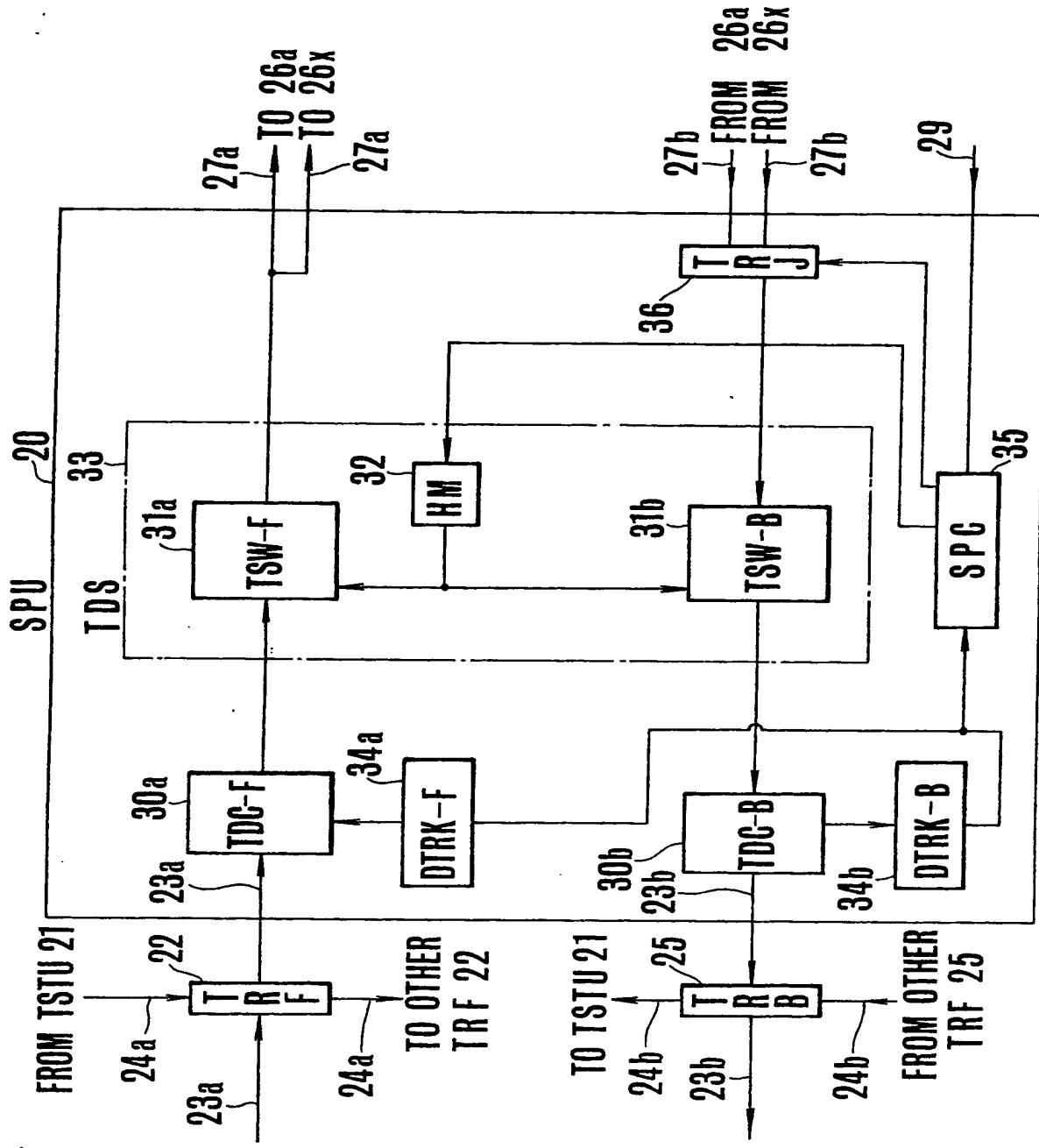
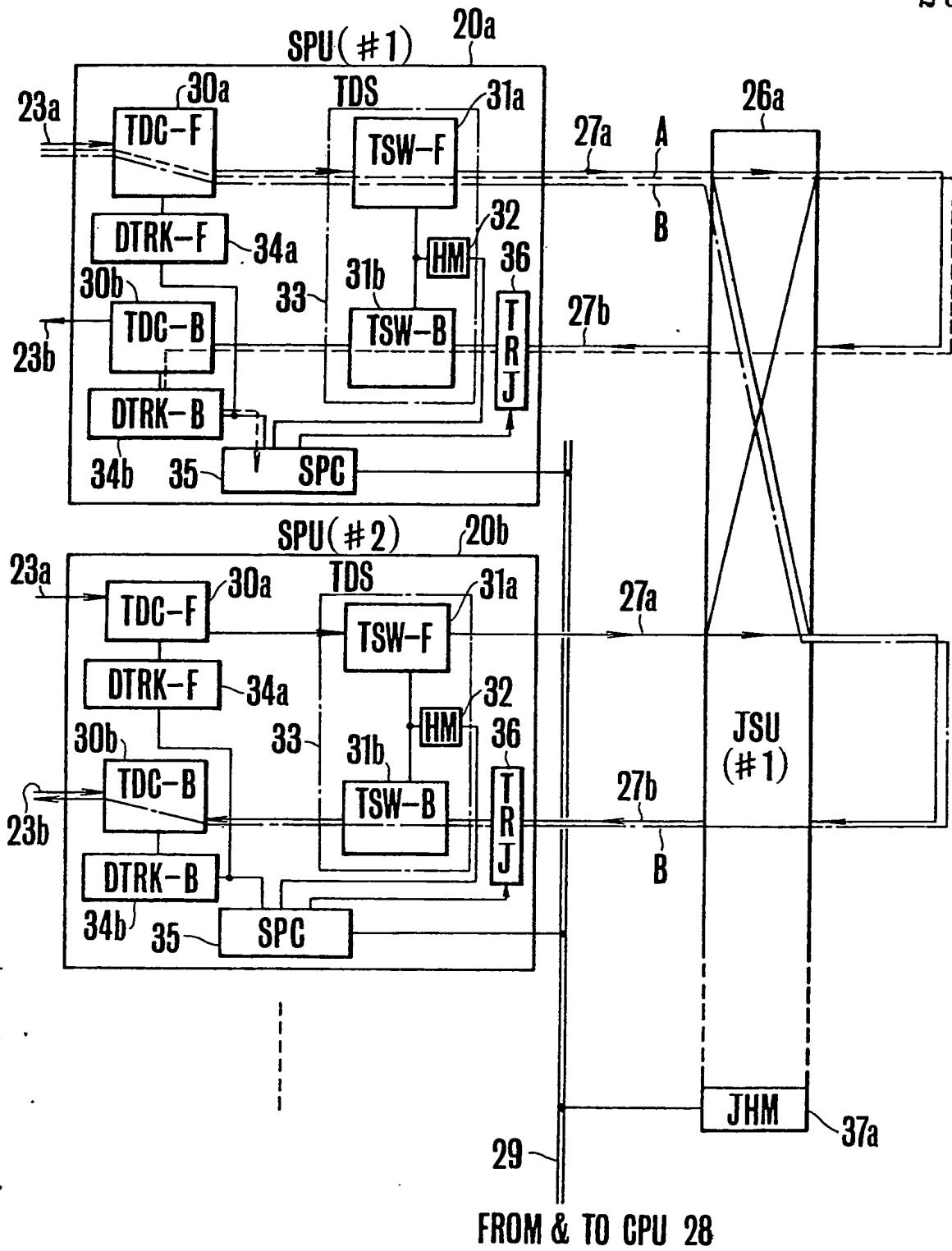


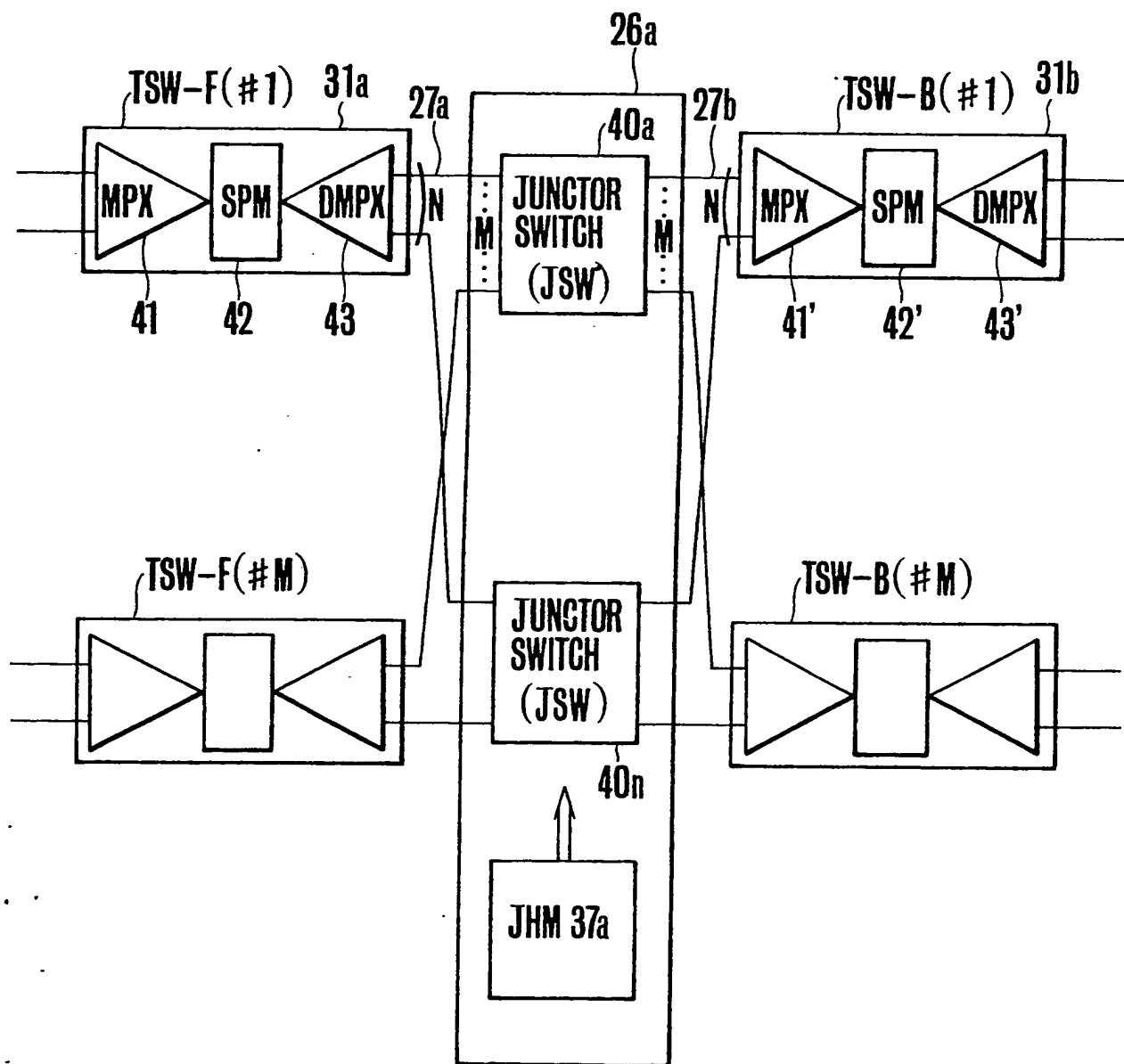
FIG.4

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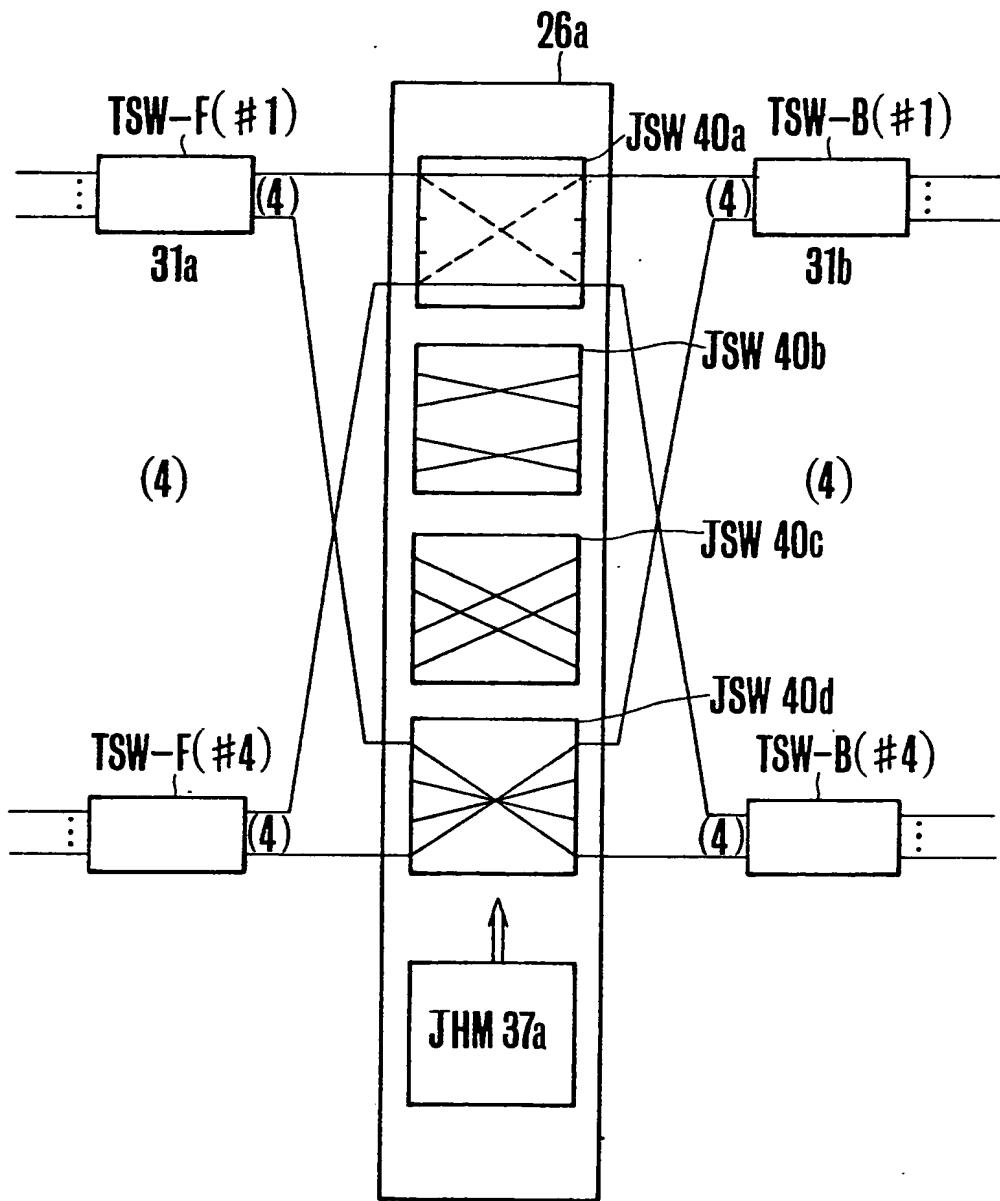
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FIG.5



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FIG.6



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FIG. 7

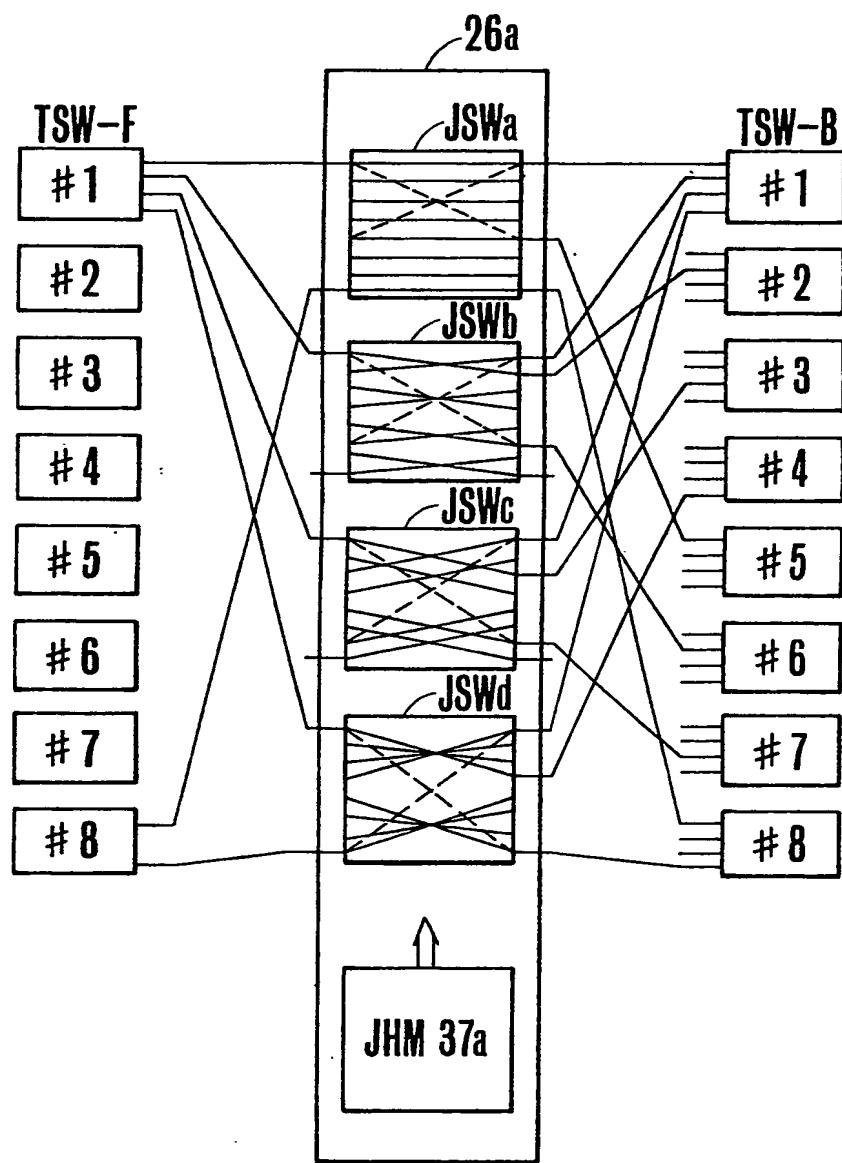
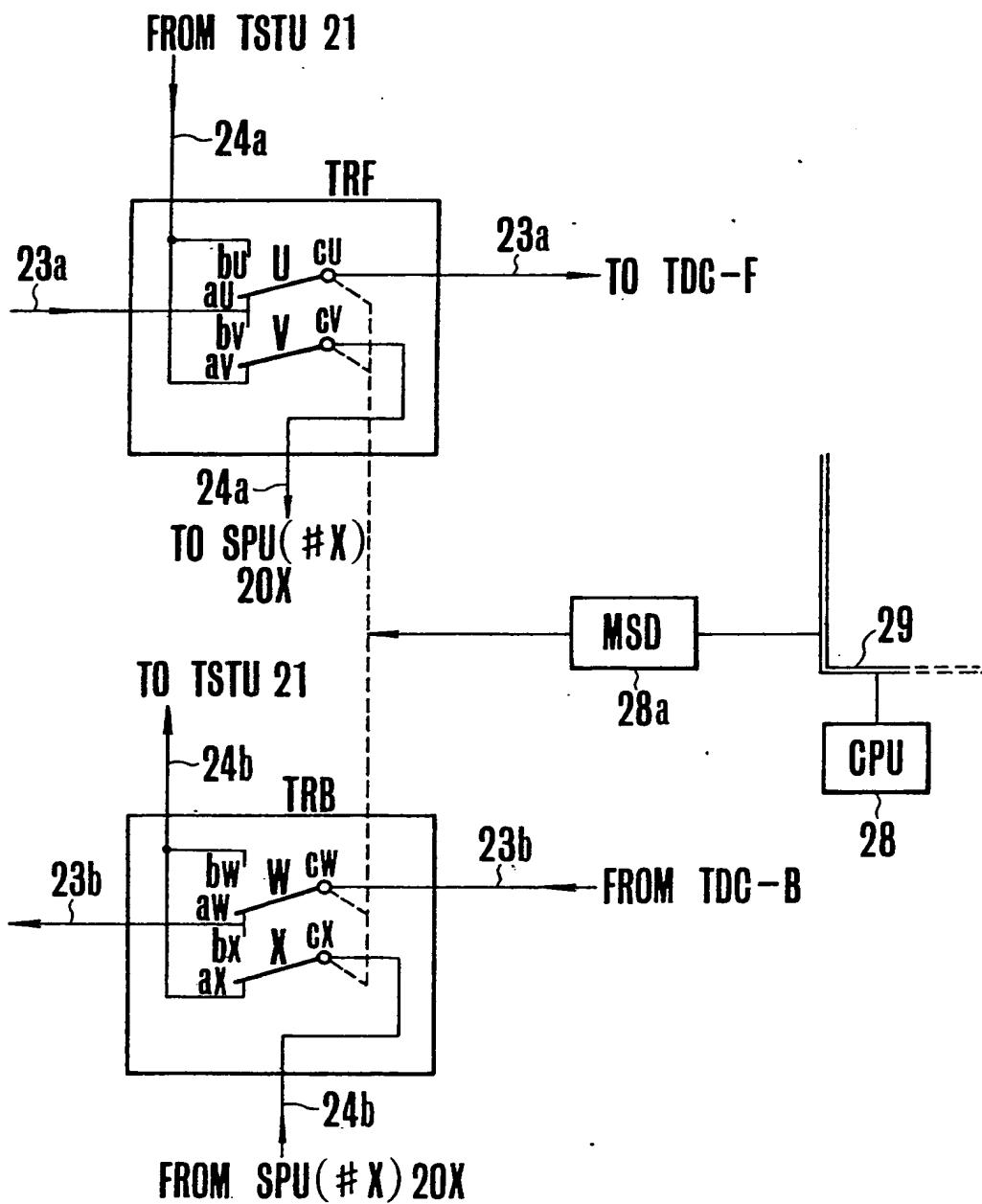


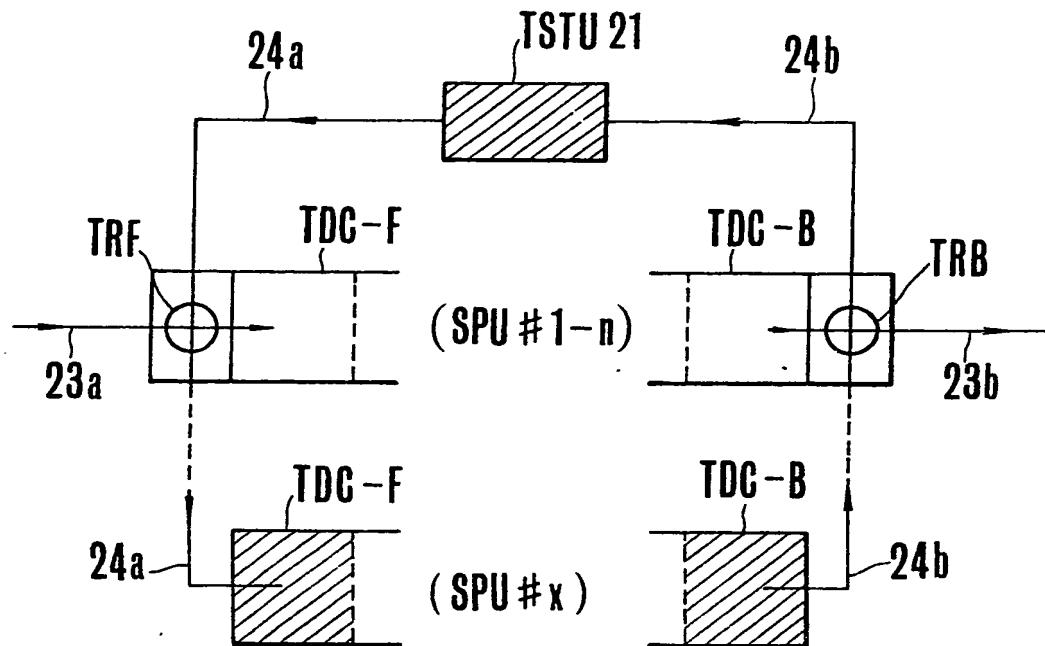
FIG.8

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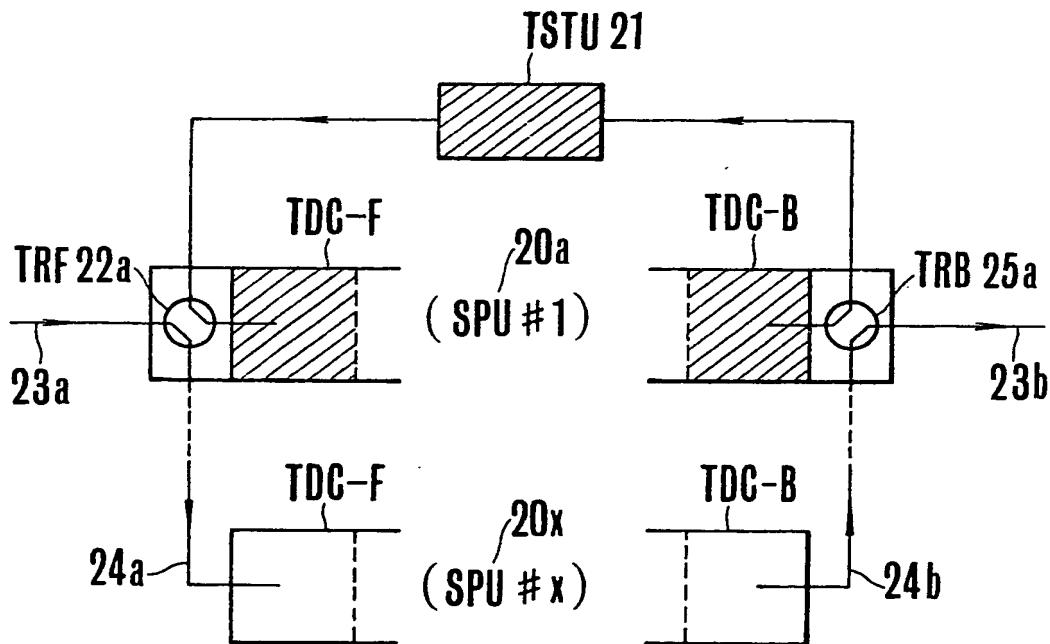


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F I G.9 A



F I G.9 B



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FIG.10

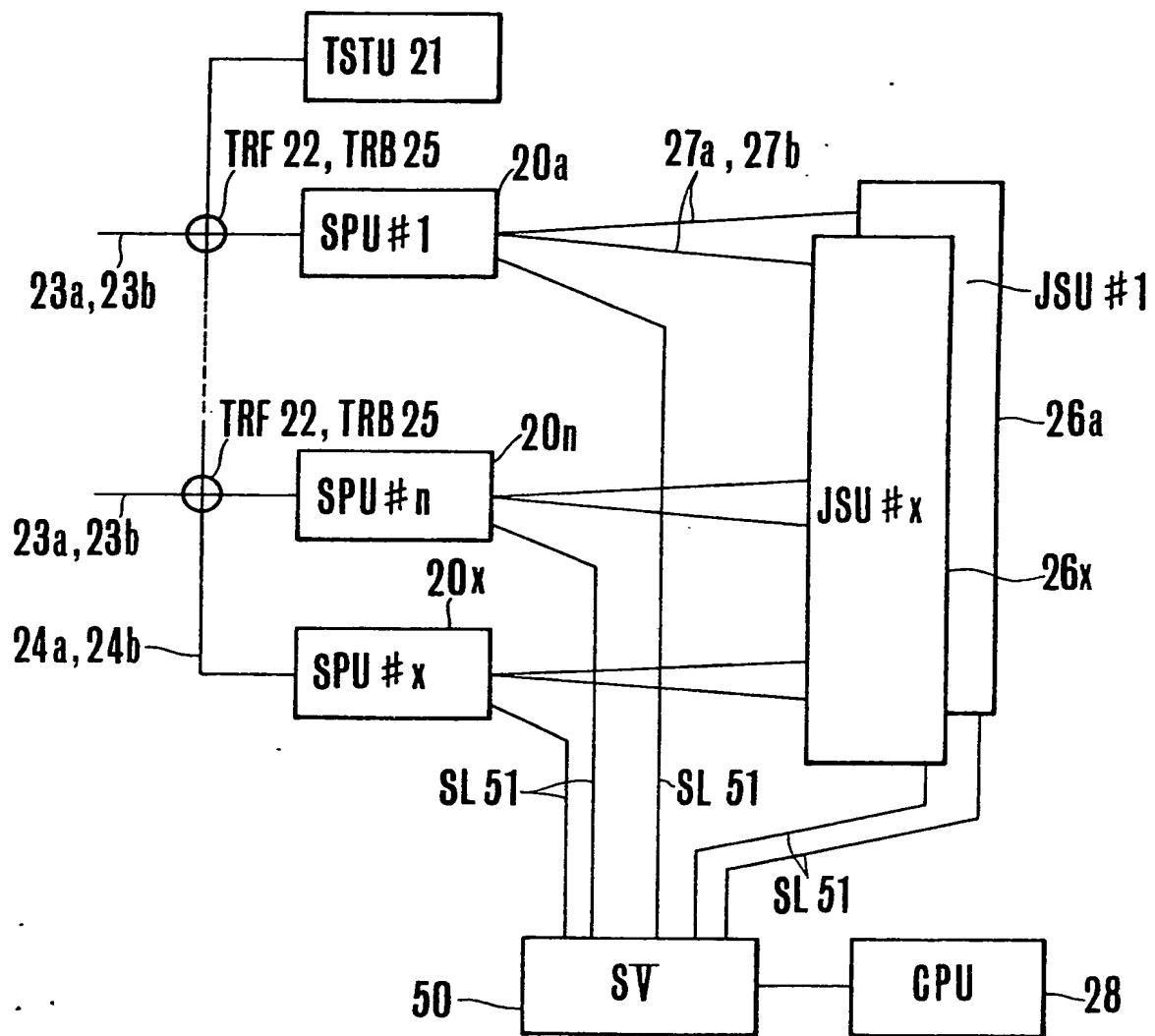
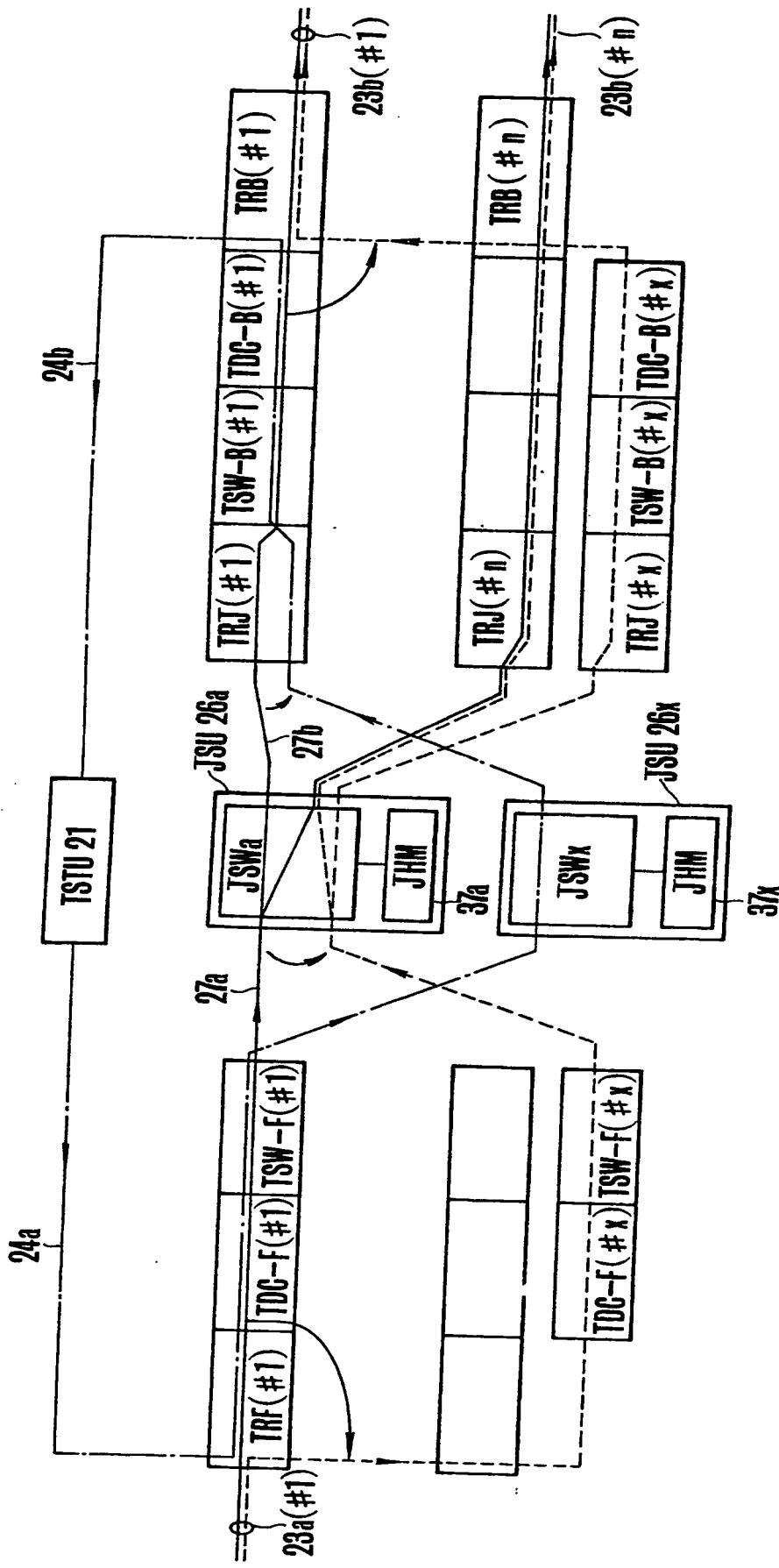


FIG.11



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F I G.12

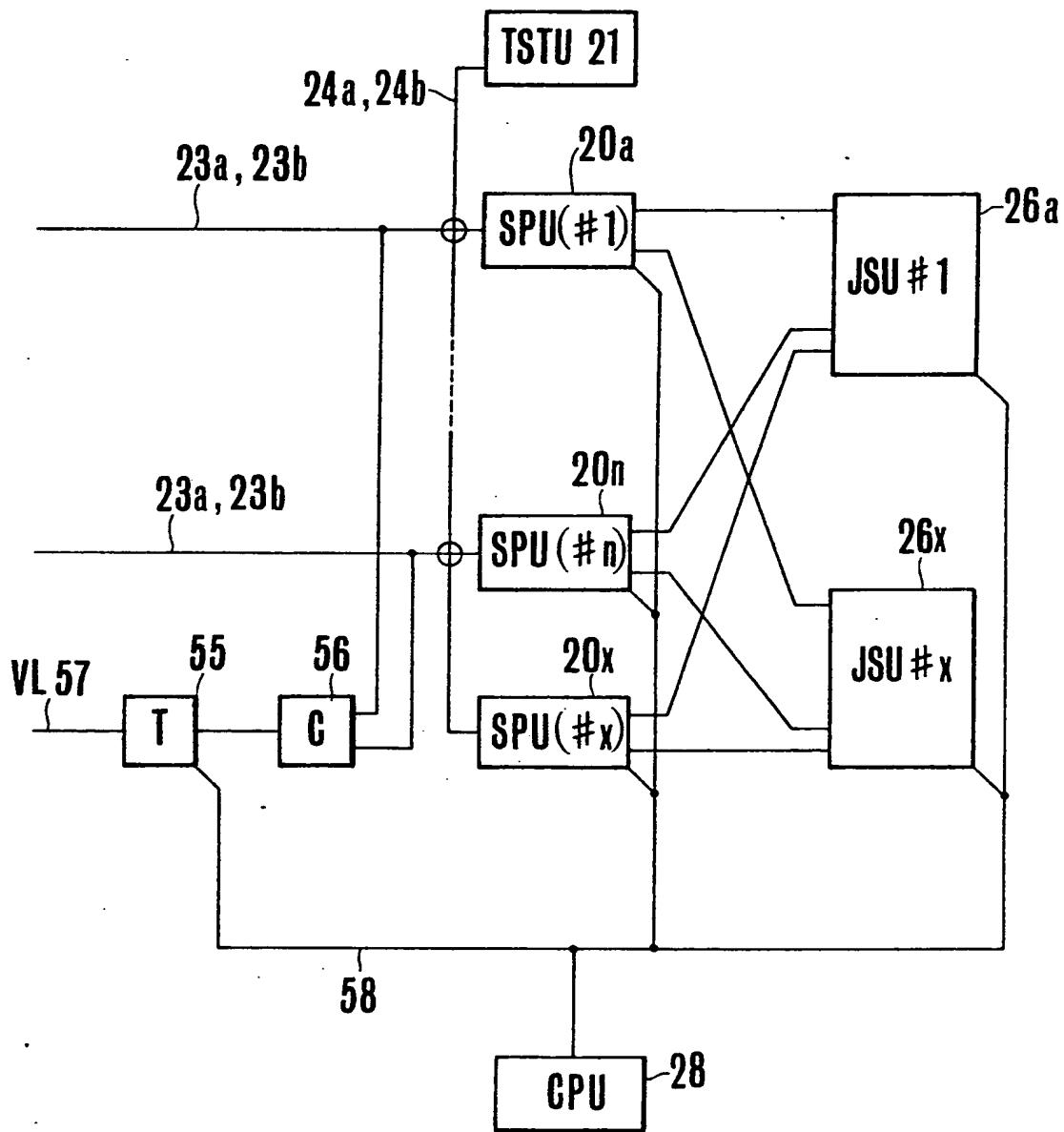
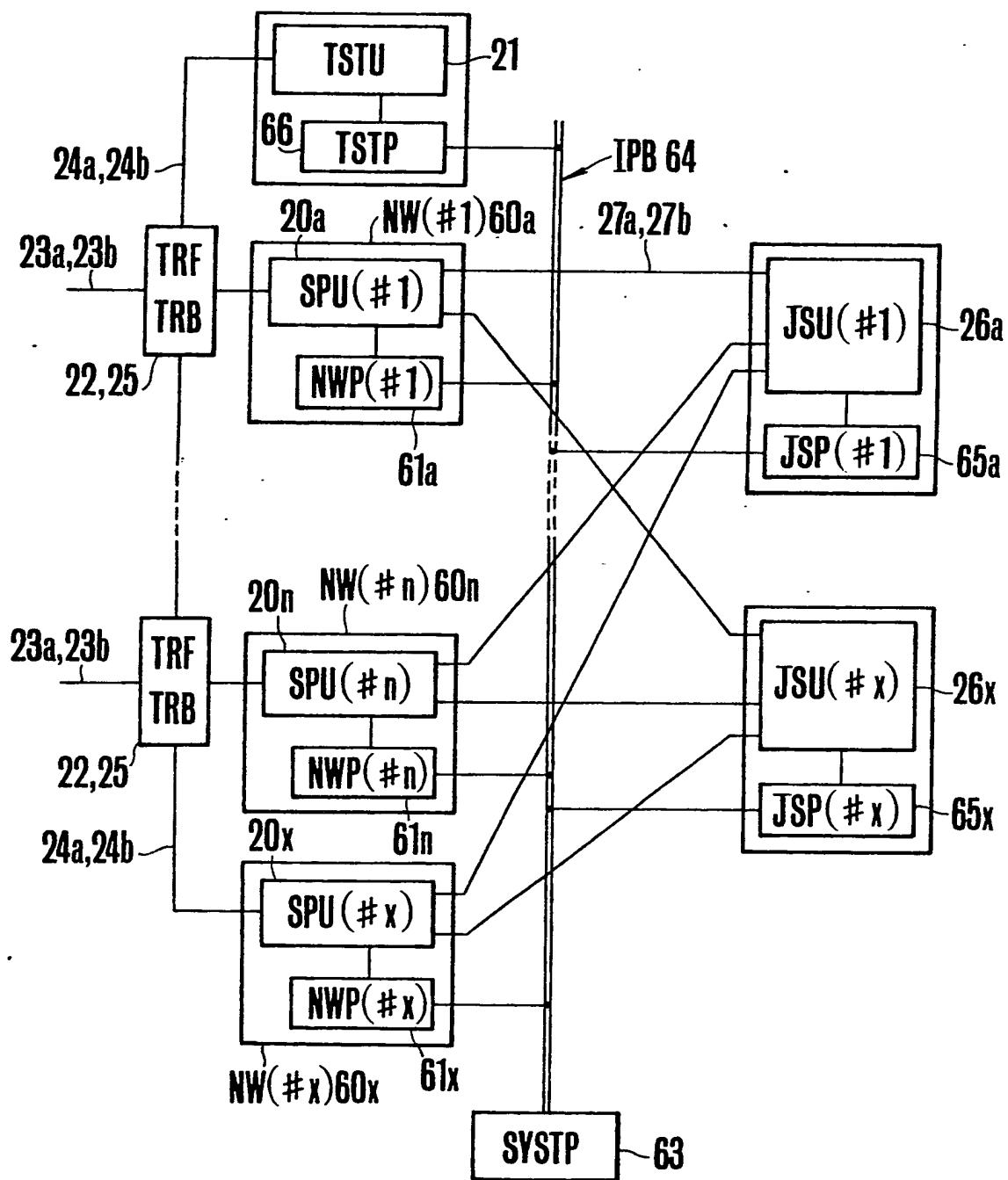


FIG.13

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FIG.14

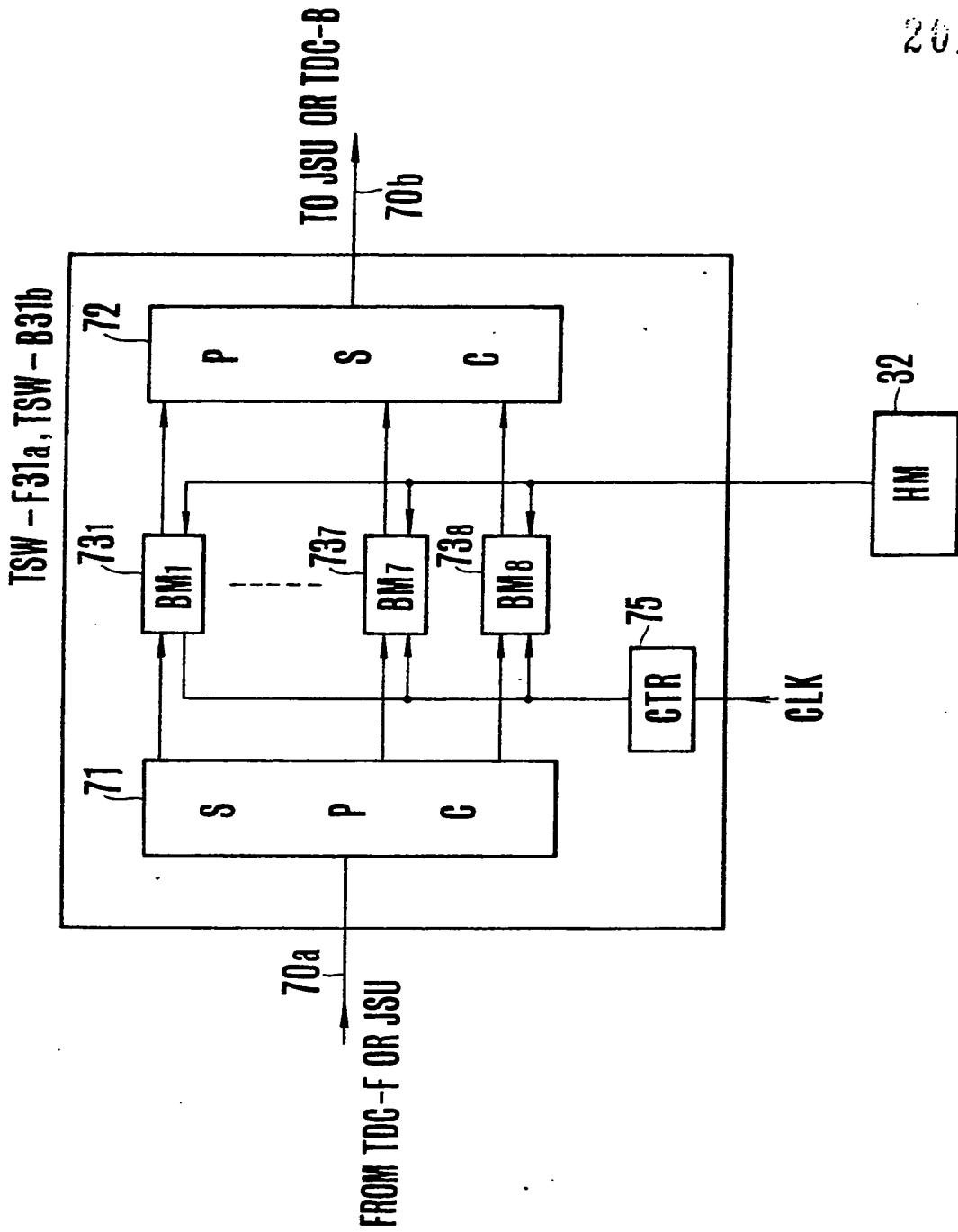
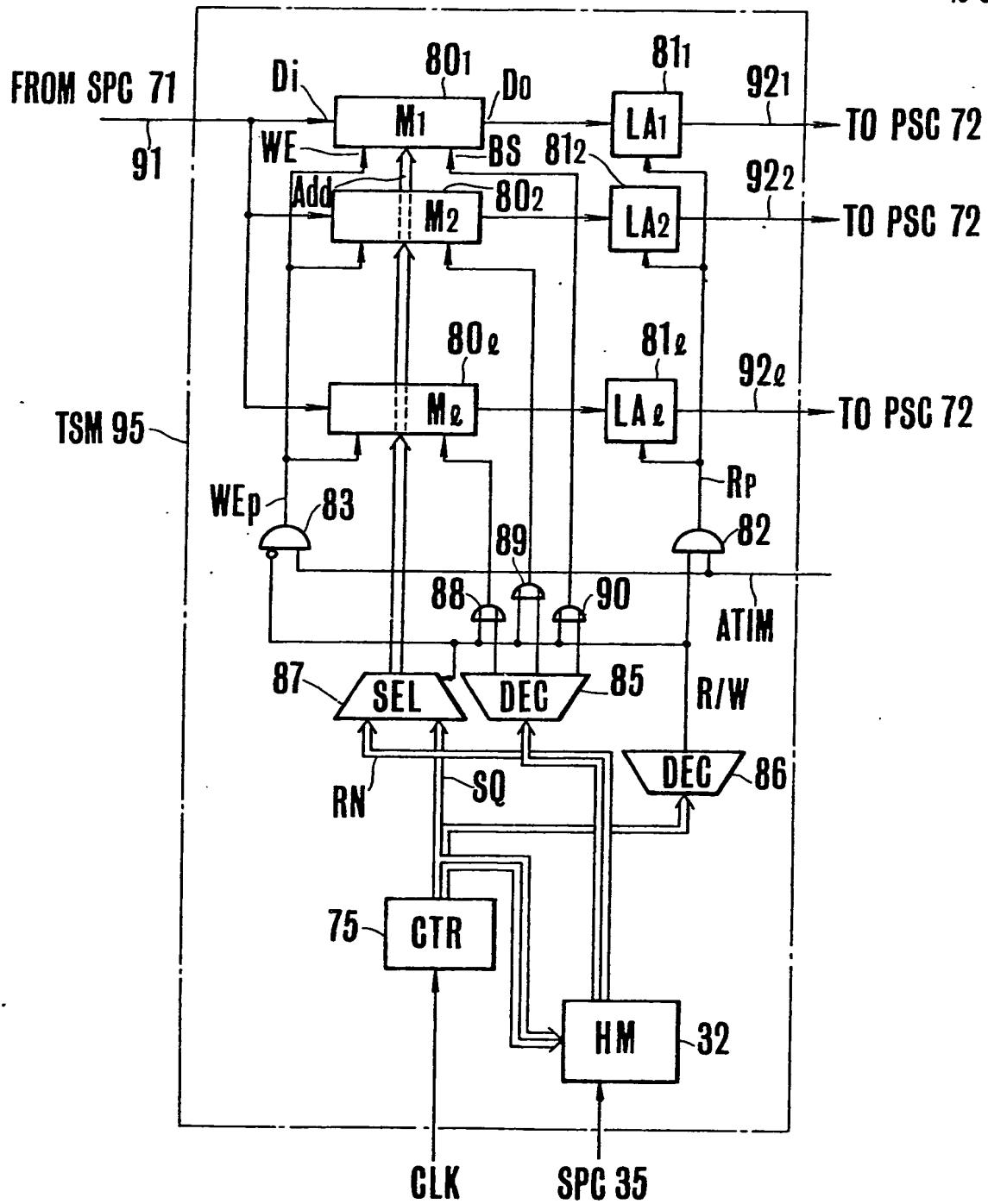


FIG. 15

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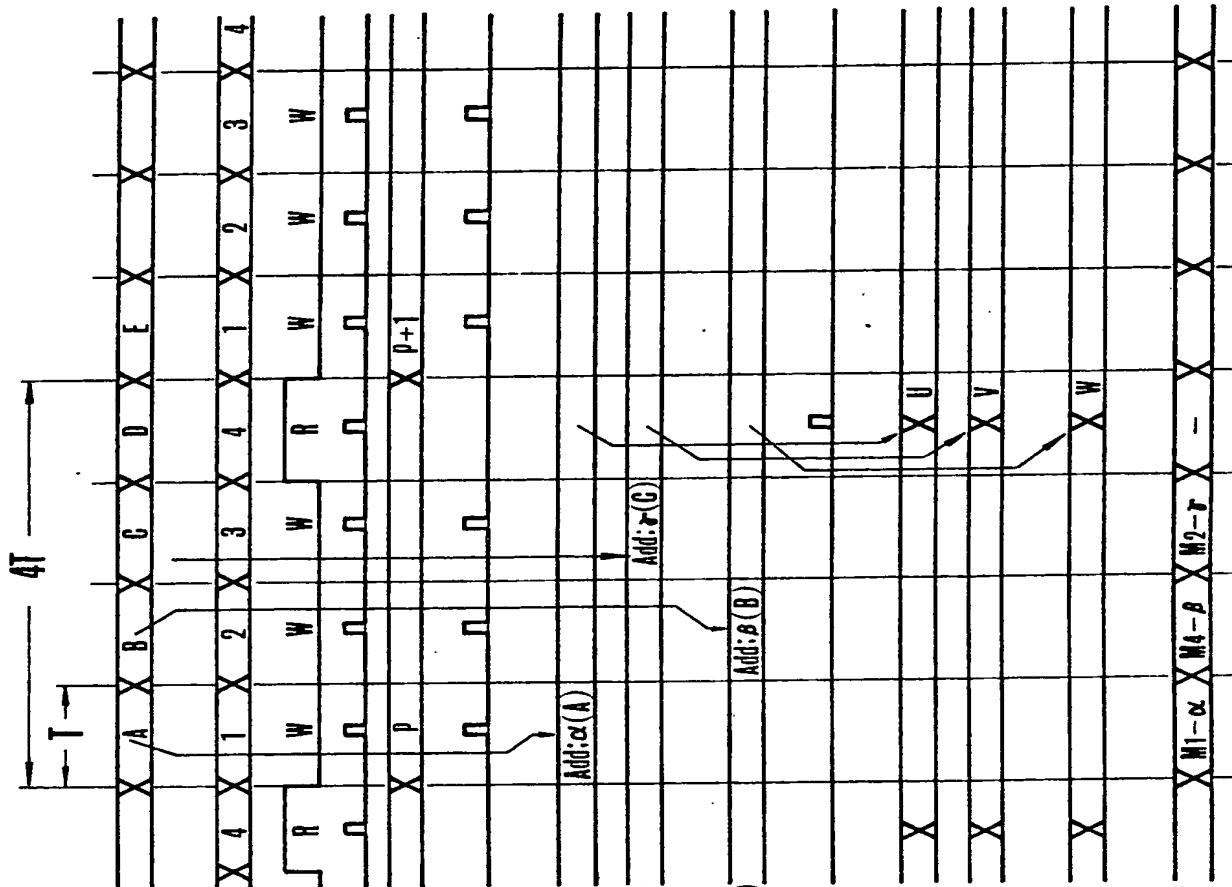


FIG. 16 A

FIG. 16 B

FIG. 16 C

FIG. 16 D

FIG. 16 E

FIG. 16 F

FIG. 16 G

FIG. 16 H

FIG. 16 I

FIG. 16 J

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FIG.17

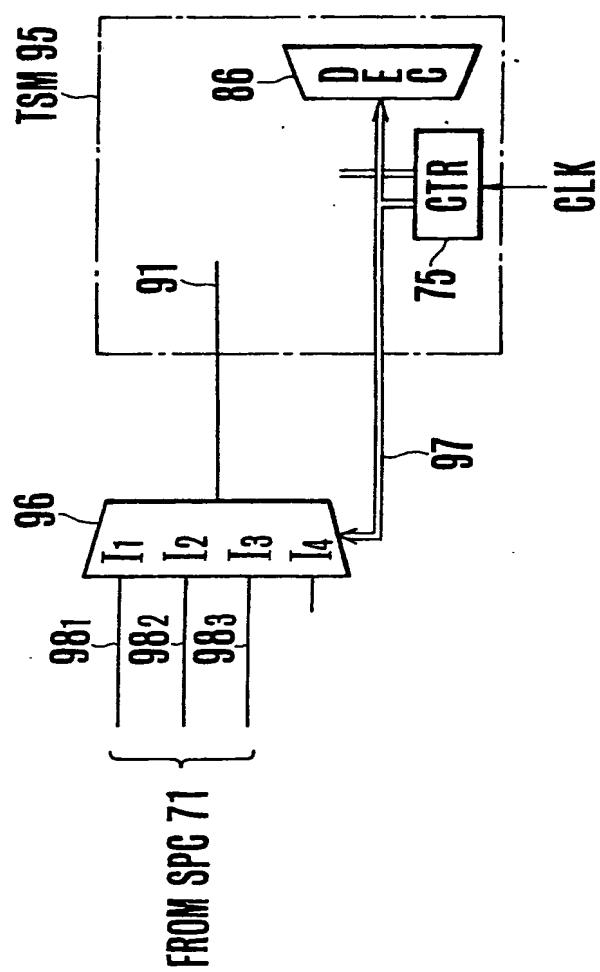


FIG.18

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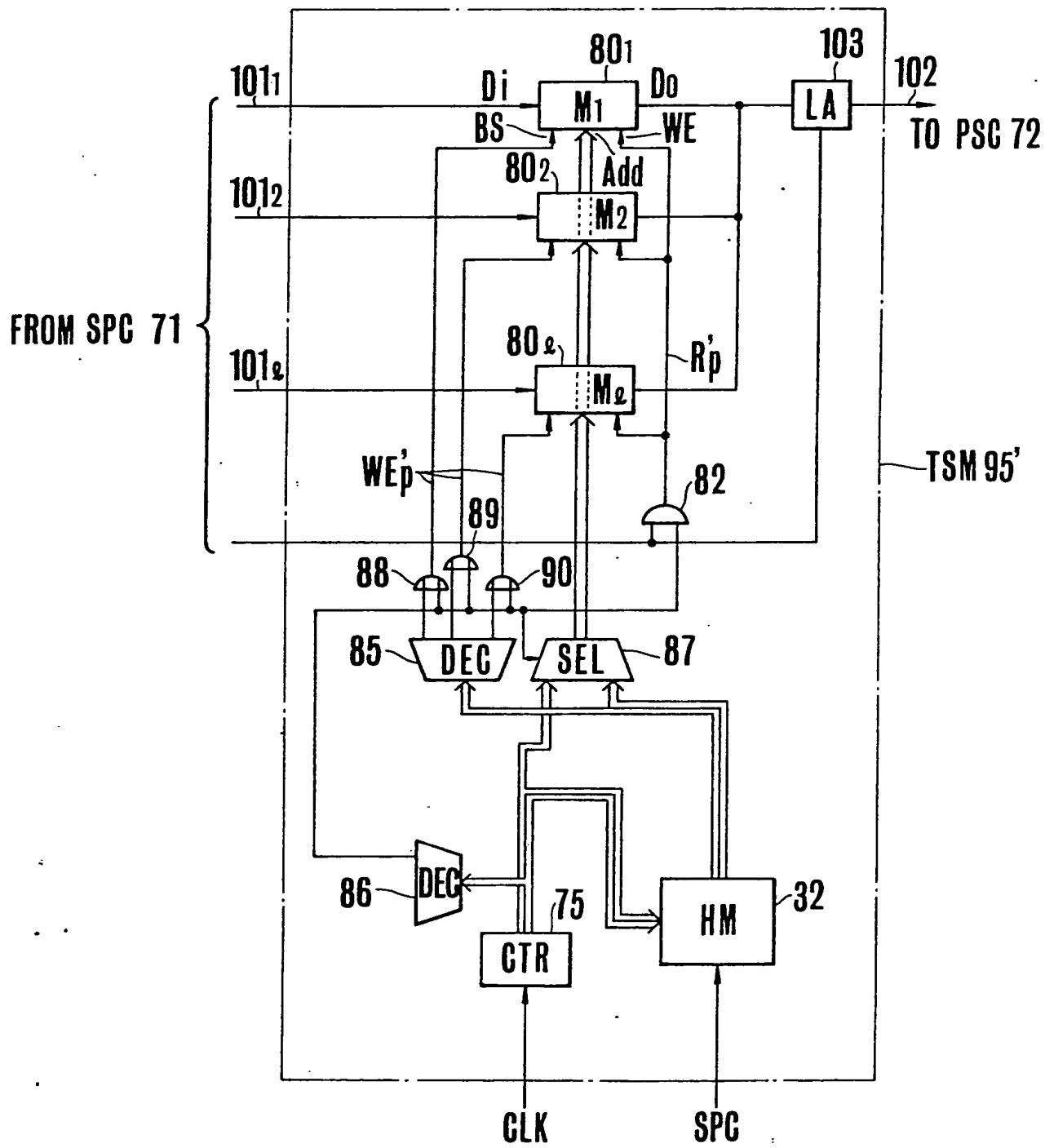
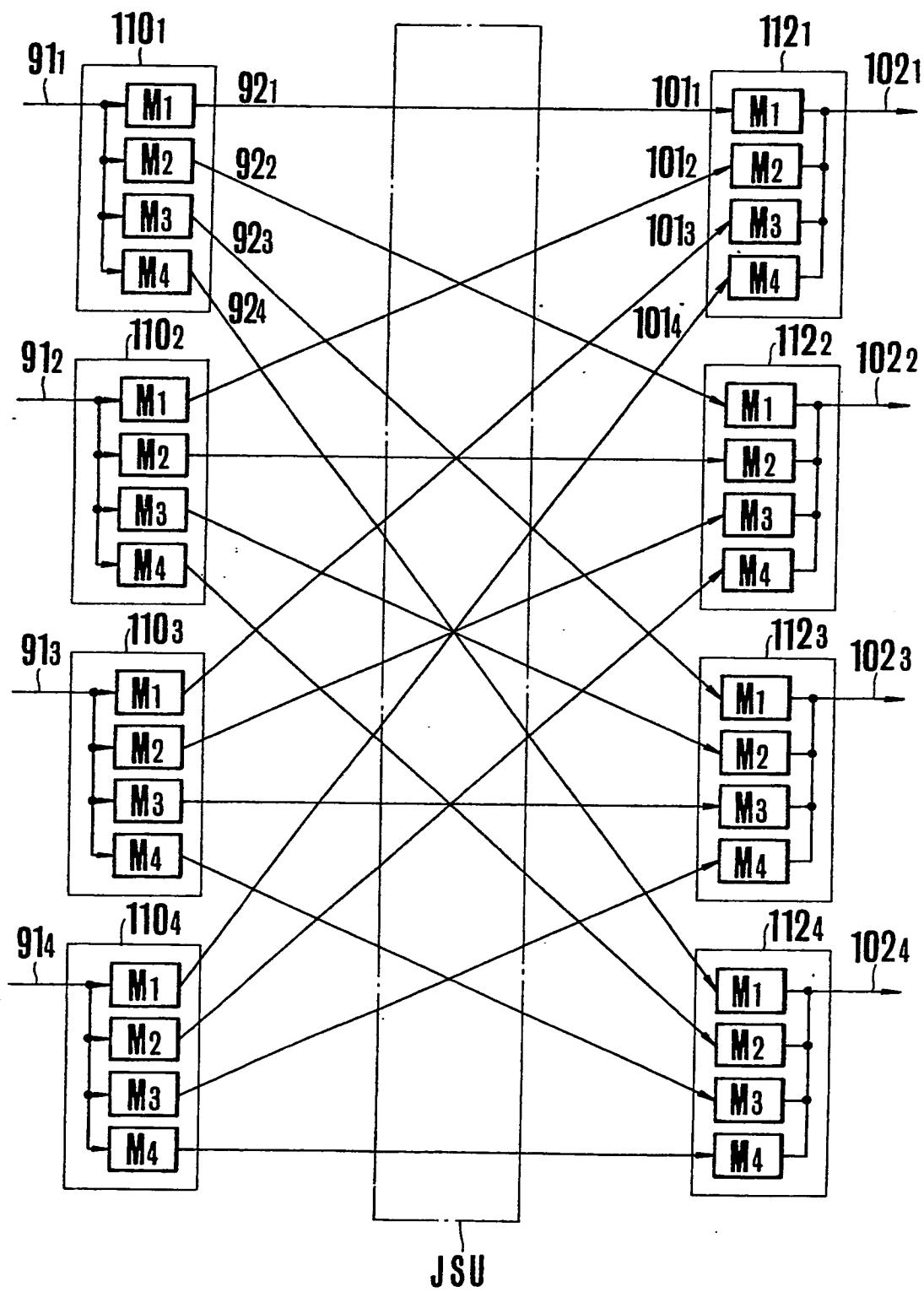


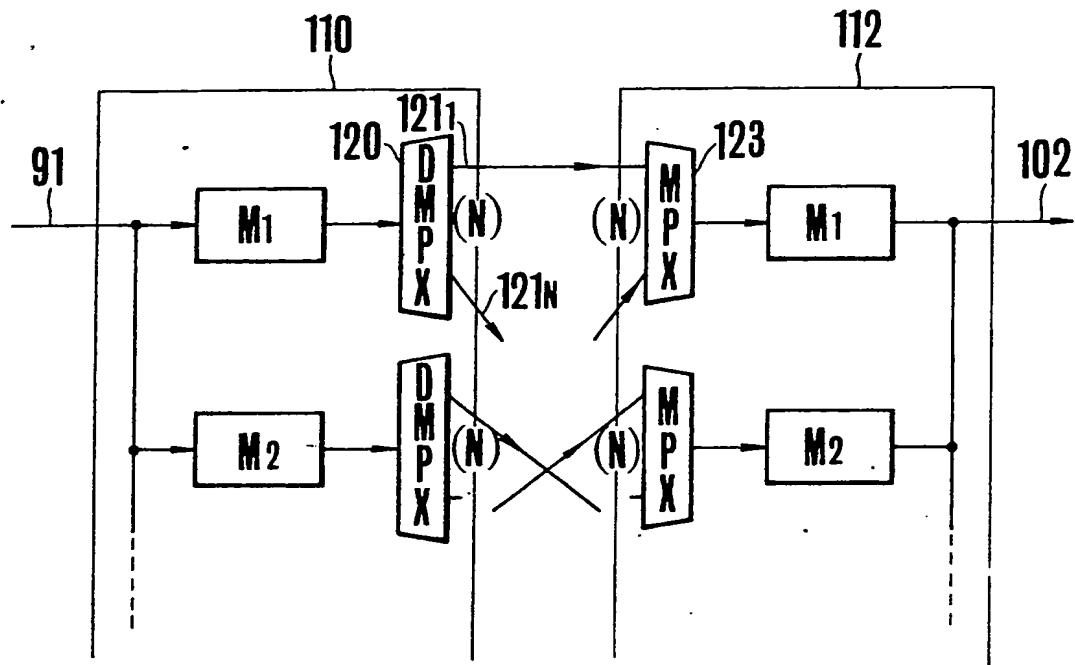
FIG.19

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F I G.20

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F I G.21

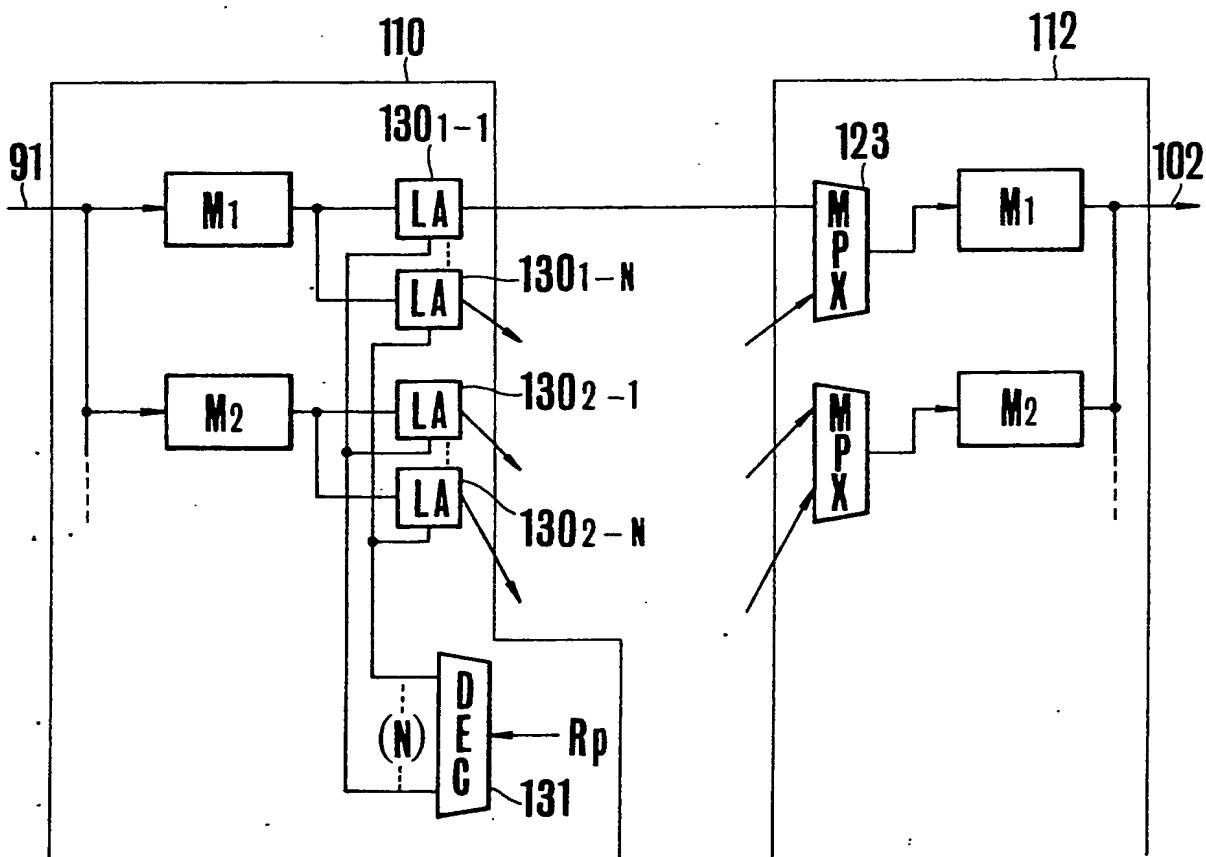


FIG.22

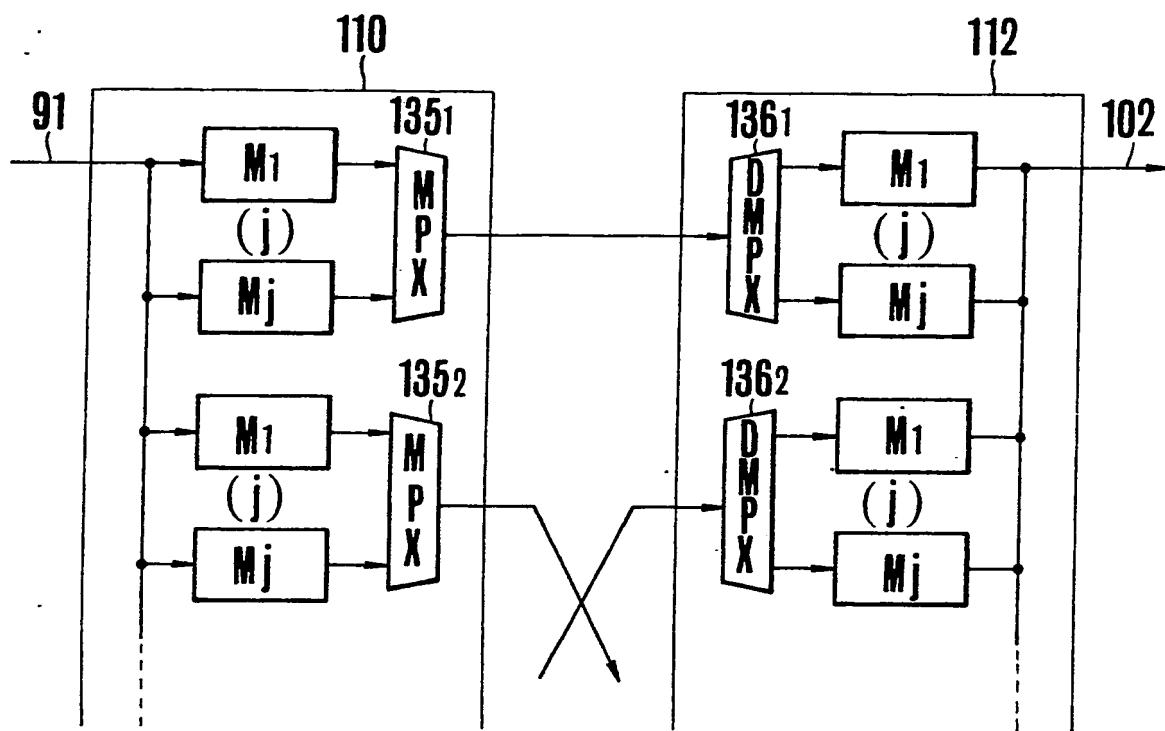


FIG.23

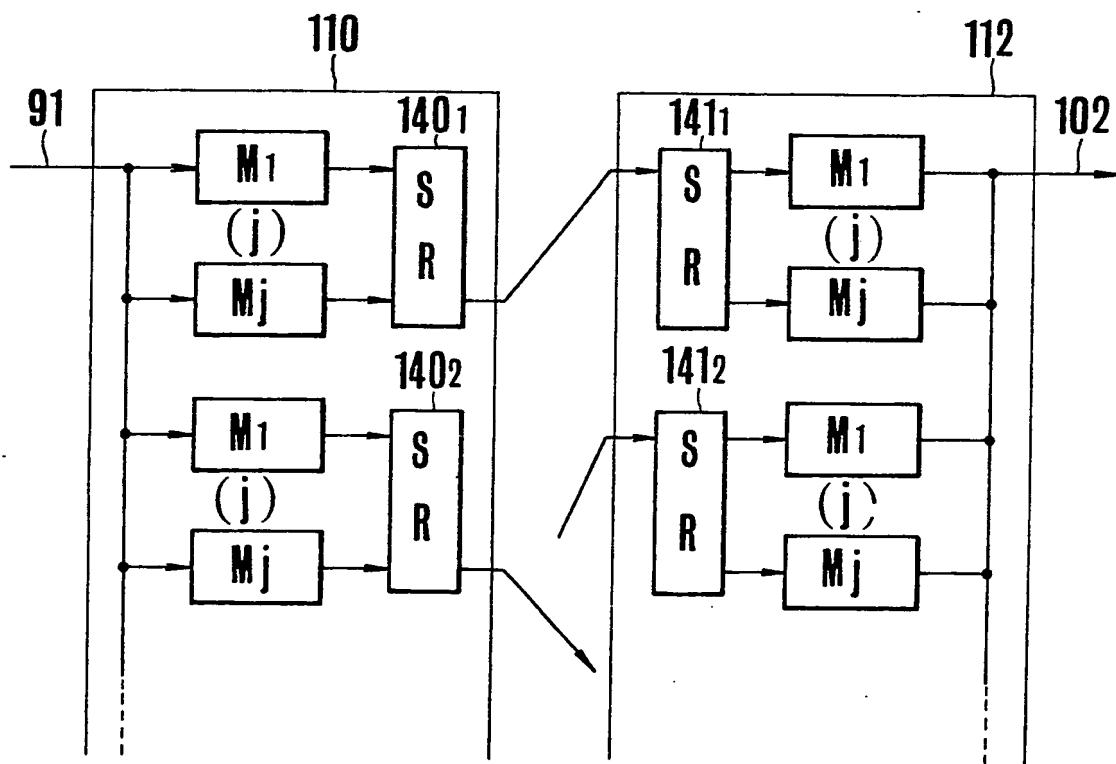


FIG.24A

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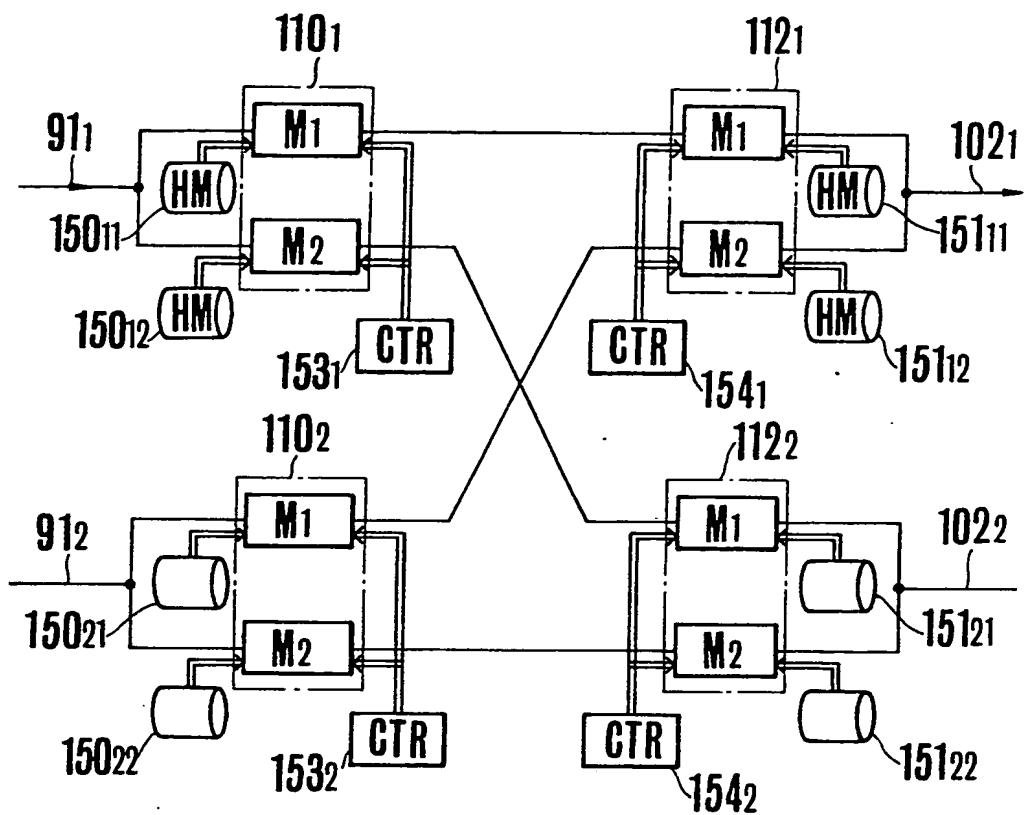
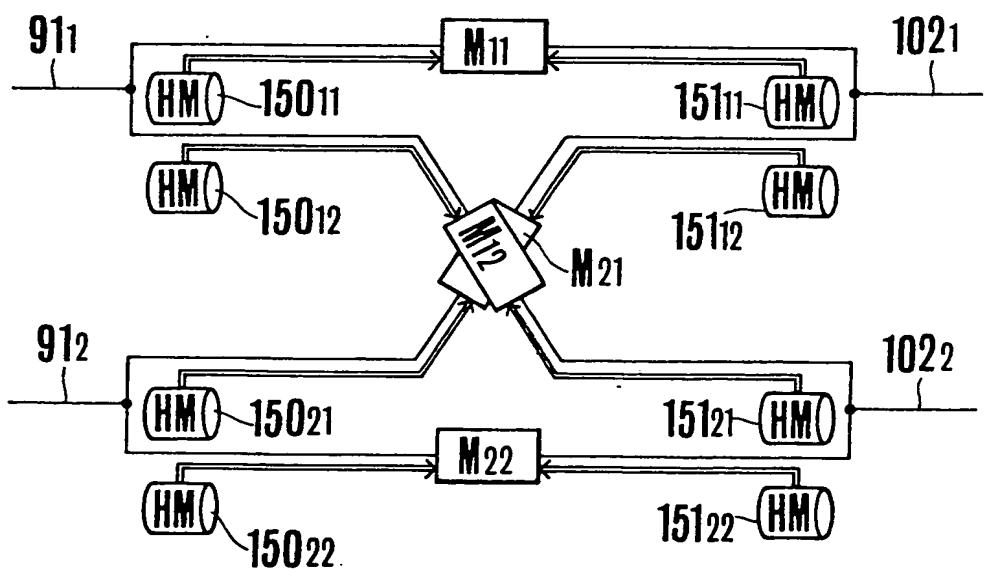
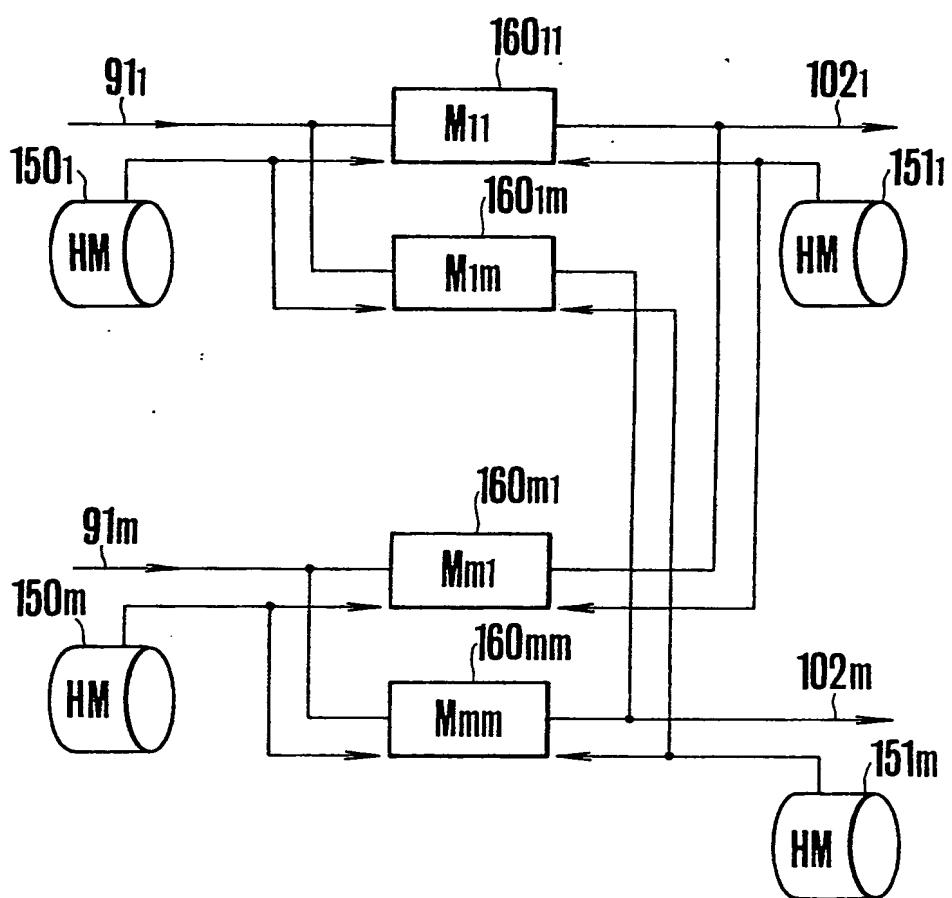


FIG.24B



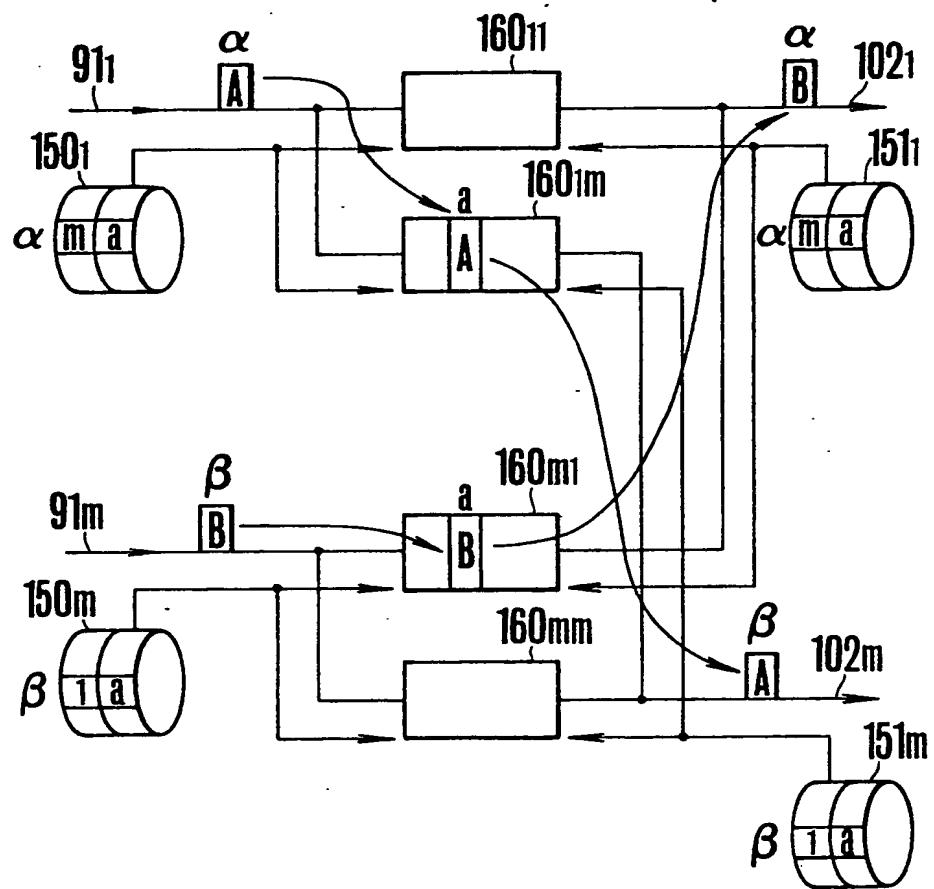
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FIG.25



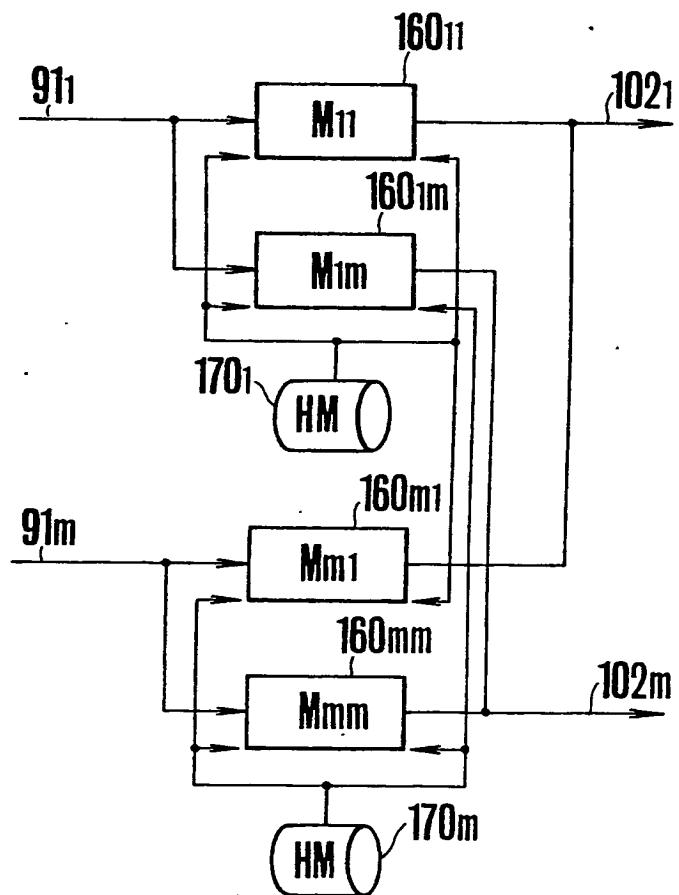
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FIG.26



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FIG.27



SPECIFICATION

Time division telephone switching systems

5 This invention relates to a time division telephone switching system.

10 A time division telephone switching system is generally constructed to exchange multiplexed signals which are sent over a plurality of incoming highways on a time division basis with time slots or channels of a plurality of outgoing highways. Such time division telephone exchange system is described, for example, in "The Bell System Technical Journal", Vol. 56, No. 7, 1977. The time division

15 telephone switching system described in this journal has a construction as shown in Fig. 1 of the accompanying drawing. Briefly stated it comprises a trunk circuit 1 (hereinafter called TRK) which receives and transmits voice signals through voice frequency

20 lines 2 (hereinafter called VL) and transmits line signals or channel associated signals, a CODEC 3 which converts analogue signals supplied from the trunk circuit 1 into digital time division multiplexed signals and a synchronizing circuit 4 (hereinafter called SYNC) which receives and transmits time division multiplexed signals over a digital line 5 and separates portions of the signals which contain the register signal and the line signal and transmits the separated portions. SYNC 4 performs to synchronize

25 the frequency and phase of the time division multiplexed signal sent over the digital line with a clock pulse of the time division telephone exchange and to multiplex and demultiplex for coinciding the time division multiplicity of the time division telephone

30 exchange and the multiplicity of the digital line. This time division telephone switching system further comprises a time division switching networks (TDNW) 6a and 6b for active mode and stand-by mode which are connected to CODEC 3 and SYNC 4

35 through changeover switches 7a and 7b respectively, and speech path controller (hereinafter called SPC) 8a and 8b for active and stand-by modes, which control the trunk circuit 1, SYNC 4 and the time division switching networks 6a and 6b. SPC 8a and 8b

40 are connected to TRK 1, SYNC 4 and TDNW 6a and 6b through changeover switches 9, 10 and 11. Central processing units (CC) 12a and 12b of the active and stand-by modes are connected to SPC 8a and 8b through a changeover switch 13 for controlling all

45 circuit elements through SPC 8a and 8b.

50 The time division telephone switching system described above receives a line signal sent over the voice frequency line 2 by TRK 1 which supplies the discriminating signal of a register signal and a channel associated signal to the active mode SPC 8a through the changeover switch 9. The voice frequency signal received by TRK 1 is supplied to CODEC 3 where it is connected into a time division multiplicity (including coincidence of the frequency

55 and phase) which accords with predetermined conditions of the time division telephone exchange in the CODEC 3 and then applied to the active mode TDNW 6a. Under the control of CC 12a, SPC 8a controls TDNW 6a in accordance with a dial register

60 signal and a line signal for transferring time division

65

multiplexed voice signals allocated to respective time slots to time slots designated by the dial register signal.

On the time slot containing the register signal and

70 the line signal of the time division multiplexed signal supplied via the digital line 5 is separated by SYNC 4 and the separated time slot signal is applied to SPC 8a. SPC 8a identifies the register signal and the line signal by judging the signal supplied from SYNC 4 to

75 control the time division switching network 6a under the control of CC 12a thus transferring the time division multiplexed voice frequency signal allocated to respective time slots to time slots designated by the register signal.

80 Where a fault occurs in any one of the time division switching unit 6a, the speech path control equipment 8a and the central processing unit 12a, a fault supervisory circuit, not shown, actuate corresponding one of the changeover switches 7a, 7b, 9, 10, 11 and 13 for changing over the faulty unit to a stand-by mode unit.

The switching operation described above is also performed between the voice frequency line 2 and the digital line 5.

90 With the time division telephone exchange described above, since the line signal supplied through the voice frequency line 2 is transmitted and received by TRK 1, and since the line signal supplied through the digital line 5 is transmitted and received by SYNC 4, the transmission and reception of these two signals and various control signals are processed differently so that the control procedure is extremely complicated and it is necessary to install a great many number of the signal lines between the

95 many units and circuits. Accordingly, when it is desired to expand or contract the telephone network of such time division switching system it is necessary not only to rearrange a large number of control lines but also to change various control procedures.

100 Accordingly, it is the principal object of this invention to provide an improved time division telephone switching system capable of economically and readily increase or decrease the switching network capacity.

105 Another object of this invention is to provide an improved time division telephone switching system capable of constructing not only the hardware but also the software utilized to control the speech path as modules.

110 Still another object of this invention is to provide a time division telephone switching system capable of decreasing the amount of job as well as the amount of program processing not only when faults occur but also during a network growth job.

115 A further object of this invention is to provide a simplified time division telephone switching system capable of decreasing the number of such components as a junctor switch holding memory device, and the amount of controls executed by these components.

120 A still further object of this invention is to provide a time division telephone switching system wherein shut down of the entire system can be prevented even when a dual or triple fault occurs.

125 Another object of this invention is to provide a

130

novel time division telephone switching system capable of economically increasing the capacity of the time division speech network.

According to this invention, these and further objects can be accomplished by digitally processing the transmission and reception of the line signals into and out of the time division telephone switching system with a digital trunk circuit and by assembling the digital trunk circuit, the time switch and the speech path control equipment into a speech path unit of a definite capacity. The speech path unit is constructed as a module so as to increase or decrease the switching network capacity by combining a plurality of such module like a building block structure.

According to this invention these and further objects can be accomplished by providing a time division multiplexed telephone switching system comprising a plurality of speech path units, a junctor switch unit for interconnecting the plurality of speech path units, a central processing unit for effecting an overall control of the speech path units; each speech path unit comprising a time switch for exchanging a time division multiplexed signal; digital trunk circuit means which processes a channel associated signal containing a register signal identification and a line operating state; and a speech path control equipment which is connected to receive and transmit a control signal between the time switch, the digital trunk circuit and the central processing unit, the junctor switch unit establishing connections and reconnections between respective speech path units by treating a plurality of time slots as one group.

Further objects, advantages and organization of the invention can be more fully understood from the following detailed description taken in conjunction with the accompanying drawings in which:

Fig. 1 is a block diagram showing one example of a prior art time division telephone switching system;

Fig. 2 is a block diagram showing one embodiment of the time division telephone switching system according to this invention;

Fig. 3 is a block diagram showing the detailed construction of the speech path unit shown in Fig. 2;

Fig. 4 is a block diagram useful to explain the switching operation of the telephone switching system of this invention by utilizing the speech path unit shown in Fig. 3;

Fig. 5 is a connection diagram showing the connections between M speech path units and a junctor switch unit;

Fig. 6 is a connection diagram of the circuit shown in Fig. 5 where M=4;

Fig. 7 is a connection diagram of the circuit shown in Fig. 5 where M=8;

Fig. 8 is a connection diagram of a changeover switch for explaining a redundant changeover performance;

Fig. 9A and 9B are connection diagrams for explaining the redundant changeover performance of the changeover switch shown in Fig. 8;

Fig. 10 is a block diagram showing a modified embodiment of this invention incorporated with a fault supervisory device;

Fig. 11 is a block diagram useful to explain a redundant changeover performance and the operation of the junctor switch unit;

Fig. 12 is a connection diagram showing a modified embodiment of this invention wherein voice frequency line signals are transmitted;

Fig. 13 is a block diagram showing still another embodiment of this invention in which processors distributed among speech path units, junctor switch units, etc.;

Fig. 14 is a block diagram showing the detailed construction of the time switch;

Fig. 15 is a block diagram showing still another modification of this invention in which the buffer memory shown in Fig. 14 is divided further;

Fig. 16 is a timing chart useful to explain the operation of the time switch module shown in Fig. 15;

Fig. 17 is a block diagram showing a modification of the system shown in Fig. 15;

Fig. 18 is a block diagram showing still further modification of the system shown in Fig. 15;

Fig. 19 is a connection diagram in which two stage time switches are constructed by dividing the time switch memory shown in Figs. 15 and 18;

Figs. 20, 21, 22 and 23 are connection diagrams respectively showing various modifications of the system shown in Fig. 19;

Figs. 24A and 24B are connection diagrams useful to explain the manner of decreasing the time switch memories shown in Fig. 19;

Fig. 25 is a block diagram useful to explain in detail the construction of the system shown in Fig. 24B;

Fig. 26 is a connection diagram useful to explain the operation of the system shown in Fig. 25; and

Fig. 27 is a block diagram showing a modification of the system shown in Fig. 25 which is incorporated with a pair control.

Fig. 2 is a block diagram showing the basic construction of the time division telephone switching system according to this invention which comprises active mode speech path units (SPU) 20a-20n, a stand-by speech path unit 20x, the units 20a-20n and 20x being integrated into a unit having a predetermined switching network capacity, a test unit 21 (TSTU) for testing the speech path units 20a-20n and 20x, and incoming transfer switches (TRF) 22a-22n which are respectively provided at cross-overs between incoming highways 23a of respective speech path units 20a-20n and the maintainance incoming highway 24a connected between the test unit 21 and the speech path unit 20x, and outgoing transfer switches (TRB) 25a-25n provided at respective cross-overs between the outgoing highway 23b of respective speech path units 20a-20n and the maintainance outgoing highway 24b extending between the speech path unit 20x and the test unit 21; active and stand-by mode junctor switch units (JSU) 26a and 26x which connect as a unit for a number of time slots between the speech path units 20a-20n via

junctor highways 27a and 27b; and a central processing unit (CPU) 28 which sends out a control signal through a control signal bus line 29 for performing the overall control of speech path units 20a-20n and 20x, the test unit 21, and the junctor switch units 26a and 26b, the analysis of various data at the time of

115 120 125 130

115 120 125 130

fault and test and the transfer instruction of incoming and outgoing transfer switches 22a-22n and 25a-25n through the maintainance signal distributing unit (MSD) 28a, which operates the transfer switches described above under the control of the central processing unit 28. Although, each of the incoming and outgoing highways 23a and 23b is represented by a single line, actually it comprises a plurality of lines acting as a highway for transmitting time division multiplexed digital signals. Thus, these incoming and outgoing highways 23a and 23b are connected to a plurality of CODECs 3 and to a plurality of synchronizing circuits 4. It should be understood that the time division multiplexed digital signal contains such multiplexed control informations necessary to effect exchange connection processing as the register signal and the line signal in addition to the voice signal (allocated to idle time slots, for example).

20 In the time division telephone switching system constructed as above described, the digitalized voice signal supplied through the incoming highway 23a is exchanged, both in space and time, by the speech path units 20a-20n and by the junctor switch unit 26a under the control of the central processing unit 28 and then sent to a CODEC or a synchronizing circuit, not shown, through the outgoing highway 23b. As will be described later in detail, each one of the speech path units 20a-20n contains means for analyzing and identifying such digitalized control signals and line signals so that the speech path unit and the junctor switch unit execute the control for ordinary time division switching operation. Consequently, the central processing unit 28 is required a 35 perform only the overall control of switch path units 20a-20n and 20x.

For this reason, even when the number of the speech path units is increased or decreased like a building block structure, it is only necessary to 40 slightly modify the junctor switch unit 26a. Because a portion for analyzing and processing such control signals as the register signal and line signal is distributed among various speech path units.

When a fault occurs in the speech path unit 20a, 45 for example, in response to a fault detection signal supplied from a conventional fault supervisory circuit, not shown, the central processing unit 28 controls through the maintainance signal distributing unit 28a, the incoming and outgoing transfer switches 22a and 25a so as to exchange the speech path unit 20a with the stand-by speech path unit 20x. Thereafter, the telephone switching operation is continued by using the speech path unit 20x. As a result of the transfer operation of the incoming and outgoing transfer switches 22a and 25a the maintainance 55 incoming and outgoing highways 24a and 24b which have been connected to the test unit 21 for testing the stand-by speech path unit 20x would be connected to the faulty speech path unit 20a. Now the 60 test unit 21 can test the speech path unit 20a which has been disconnected from the main switching system owing to the occurrence of a full and the test result is supplied to the central processing unit 28 through the control signal bus line. Having completed the description regarding the construction 65

and operation of the block diagram shown in Fig. 2, the detail of the construction of the speech path units 20a-20n and 20x will be described in detail in the following.

70 Fig. 3 shows the detail of the speech path unit (SPU) 20 shown in Fig. 2 in which corresponding elements are designated by the same reference numerals. In Fig. 3, 30a and 30b show forward and backward time division speech path connecting equipments (TDC-F, TDC-B) connected to the incoming transfer switches (TRF) 22 and the outgoing transfer switches (TRB) 25 respectively, 31a and 31b show time switches (TSW-F, TSW-B) respectively connected to the time division speech path connecting equipments 30a and 30b, and 32 represents a holding memory circuit (HM) for controlling the storing or reading out position (timing) of the time switches 31a and 31b. The time switches 31a, 31b and the holding memory circuit 32 constitute a time 85 division switching equipment (TDS) 33. The forward time division speech path connecting equipment (TDC-F) 30a is connected to the incoming transfer switch (TRF) 22 to receive the digital signal sent over the incoming highway 23a and to match the timing 90 with the switching system standard clock pulse for performing the time division switching operation. If desired, for the purpose of constructing the time switch 31 with an economical low speed memory device, the forward time division speech path connecting equipment 30a is constructed to perform a portion of the series-parallel conversion and the multiplexing conversion. The time switch (TSW-F) 31a is constructed to receive and store the time division multiplexed signals from the forward time division speech path connecting equipment (TDC-F) 30a and to operate the time switch under the control of the holding memory circuit (HM) 32. On the other hand, the secondary time switch (TSW-B) 31b is connected to receive and store the signals from the 100 junctor switch unit (JSU) 26 for effecting the switching operation under the control of the holding memory circuit.

Generally, these time switches 31a and 31b operate to receive the signals sent from the incoming 110 highway and store the multiplexed signals in speech path memory devices comprising several random access memories (RAM). When the stored signals is read out by being addressed by the holding memory circuit they are sent out to the outgoing highway.

115 Reference characters 34a and 34b designate digital trunk circuits (DTRK-F, DTRK-B) which receive and identify (or operate reversely) such control signals as the register signal and the line signal which have been allocated to idle channels by digital multiplex processing technique. The control signals also include such inter-office signals as a multi-frequency signal and a supervisory signal, various tone signals and test signals 35 represents a speech path control equipment (SPC) acting as an interface between 120 holding memory circuit (HM) 32, digital trunk circuits 34a and 34b, and central processing unit 28 for receiving, distributing and partially preprocessing the control signals, 36 designates a junctor transfer switch (TRJ) which selects junctor switch units (JSU) 125 130 26a are 26x shown in Fig. 2.

In the speech path unit (SPU) 20 constructed as above described, the time division multiplexed voice signal and the line signal which are supplied through the incoming highway 23a are applied to the forward time division speech path connecting equipment (TDC-F) 30a through the incoming transfer switch (TRF) 22. The forward time division speech path connecting equipment (TDC-F) 30a receives the digitalized signal for matching the timing and condition with the standard clock pulse of the switching system which is used when the time division switching operation is performed. If desired, the forward time division speech path connecting equipment 30a executes the series-parallel conversion and a portion of the multiplex switching operation for the purpose of simplifying the switching processing. The digital trunk circuit (DTRK-F) 34a supplies such control signals as the register signal and the line signal to the forward time division speech path connecting equipment (TDC-F) 30a under the control of the speech path control equipment (SPC) 35, which sends information for effecting the switching processing in the holding memory circuit (HM) 32 under the control of the central processing unit (CPU) 28. In response to the exchanged information, the holding memory circuit (HM) 22 controls the time switch (TSW-F) 31a for transferring the information to a time slot position thereby exchanging the incoming voice signal and the line signal. Since the holding memory circuit 31a is well known in the art it is considered unnecessary to describe its construction and operation.

On the other hand, the digital trunk circuit (DTRK-B) 34b digitally processes the line signals received from another offices through forward time division speech path connecting equipment (TDC-F) 30a, time switch (TSW-F) 31a, junctor switch unit (JSU) 26a (Fig. 2) and time switch (TSW-B) 31b and backward time division speech path connecting equipment (TDC-B) 30b, and sends the result of processing to the central processing unit (CPU) 28 (Fig. 2) via the speech path control unit (SPC) 35.

Fig. 4 is a connection diagram showing the inter-office line signals between two speech path units 20a and 20b and the junctor switch unit (JSU) 26a in which components identical to those shown in Figs. 2 and 3 are designated by the same reference characters.

In Fig. 4 a route A shown by dotted lines shows the path of a line signal which is sent from another offices via such digital terminating equipment as the CODEC 3 or synchronizing circuit 4 described above by utilizing a specific idle time slot of the highway 23a. The route A is used to semipermanently apply the time slot of a line signal transmitted over the highway 23a to the digital trunk circuit (DTRK) 34. Suppose now that a line signal is supplied to the digital trunk circuit (DTRK-B) 34b via this semipermanently established signal path, the digital trunk circuit (DTRK-B) 34b would receive such control signals as the register signal and the line signal and supply them to the speech path control equipment (SPC) 35 which translates and identifies the control signals by itself or under the control of the central processing unit (CPU) 28 and then, depending upon

the result thereof, performs the switching operation by controlling the time switches 31a and 31b if connection is to be established between the time slots in the speech path unit (SPU) 20a.

70 In this manner, when an input is applied to an outgoing highway containing its own speech path unit, the speech path control equipment (SPC) 35 would receive a line signal through digital trunk circuit (DTRK-B) 34b so that the speech path control equipment 35 controls the time switches (TSW-F, TSW-B) 31a and 31b through the holding memory circuit (HM) 32 by itself or under the control of the central processing unit (CPU) 28 for connecting the input to the outgoing highway 23b. The line signal to the other office is sent from the digital trunk circuit (DTRK-F) 30a through the semipermanent path.

When it is desired to connect this input to a highway contained in another highway, for example in the speech path unit 23b the speech path control equipment (SPC) 35 in the speech path unit 20b controls the holding memory circuit 32 in the speech path unit 23b under the control of the central processing unit (CPU) 28 to establish a path bounded by dot and dash lines.

80 90 In response to a control signal supplied from the central processing unit 28, a junctor holding memory circuit (JHM) 37a controls the junctor switch unit (JSU) 26a so as to establish a semipermanent connection path between speech path units. Although in the foregoing description, only the reception of the line signal from the highway 23a of the speech path unit 20a and the establishment of a one-way speech path from the highway 23a of the speech path unit 20a to the highway 23b of the speech path unit 23b were described, it should be understood that the two-way speech path can also be established.

Although the construction and operation of the junctor transfer switch (TRJ) 36 will be described hereinafter, at this stage of description it may be deemed as a through circuit.

95 The digital trunk circuit (DTRK-F) 34a of the speech path unit 23a generates a busy tone signal utilized at the time when a line is idle. As described above, it is possible to send this busy tone signal to any time slot on the outgoing highway 23b by connecting it to the highway 27b by establishing a permanent path through time switch (TSW-F) 31a and the junctor switch unit (JSU) 26a.

100 115 In this case, it is possible to send the busy tone signal by only the speech path control equipment 35 in each speech path unit 20a or 20b without awaiting the control of the central processing unit 28 thereby improving processing ability (overall efficiency) of the central processing unit 28. Since the junctor between the speech path units is semipermanently established it is possible for the speech path control equipment 35 in each speech path unit 20 to know the present junction pattern whereby the speech path connection, transmission and reception of signals, test, etc. in its speech path unit can be made readily. Accordingly, it is possible to construct not only hardwares but also softwares as modules.

120 125 Thus, when expanding the switching network capacity it is only necessary to pile up the speech path units 20 as shown in Fig. 2 just like a block building

and the expansion construction test can readily be made by using the stand-by mode junctor switch unit (JSU) 26x and test unit (TSU) 21. It is expected that various elements shown in Fig. 3 5 can be integrated into a single component block (for example, one unit, one frame) when high speed operation and miniaturization become possible as a result of advance in integrated circuit technique. With the prior art redundant structure for each 10 apparatus, it has been inevitable to increase the number of hardwares which are necessary to effect redundant switching of respective apparatus. However, by effecting redundant switching for each unit structure (speech path unit) as has been described 15 above, the defect just described can be obviated.

Fig. 5 shows the connection between M speech path units (SPU) and a junctor switch unit (JSU) in which time switches TSW-F and TSW-B which have been considered as being contained in a single 20 speech path unit (SPU) are disposed on both sides of the junctor switch unit (JSU) for the purpose of facilitating the description thereof. In Fig. 5, the junctor switch unit (JSU) is constituted by N junctor switches (JSW) 40a-40n having M incoming and 25 outgoing lines, and a junctor holding memory circuit (JHM) 37a. Each time switch (TSW-F) comprises a multiplexer circuit (MPX) 41 which multiplexes the signals from the incoming highway, a speech path memory device (SPM) 42 which stores the output signals of the multiplexer circuit 41, and a demultiplexer circuit (DMPX) 43 which distributes the output read out signals from the speech path memory device 42 on N junctor highways. The address 30 informations for the speech path memory device 42 are stored in a holding memory circuit (HM) 32 (not shown in Fig. 5) corresponding to each speech path unit (SPU). The time switch TSW-B also comprises a multiplexer 41', a demultiplexer 43', and a speech path memory device 42' which operate in the same 35 manner as the corresponding elements of the time switch TSW-F.

With this construction, the change in the junctor pattern between junctor highways 27a and 27b can be made automatically by the junctor switch unit 40 45 26a. Moreover, it is possible to decrease the number of the junctor highways extending from one time switch can be minimized (one) by multiplexing the junctor highways 27a and 27b on the time division basis thus decreasing the number of cables and 50 facilitating the expansion job.

The optimum number of the junctor highways extending from one time switch, is determined depending upon the signal speed condition on the junctor highways, the timing allowance between the 55 speech path unit 20 and the junctor switch unit 26, the number of the junctor switches and the volume of the hardware. This relationship will be described in the following with reference to a typical example.

For the sake of description, it is now assumed that 60 the number (N) of the junctor switches (JSW) is 4, and that the capacity of the matrix of each junctor switch (JSW), that is the number (M) of the junctor highways connected to the time switches (TSW) 31a and 31b are 4 and 8 respectively.

Fig. 6 shows the connection of a case wherein 65

M=4. In this case the connections of the junctor switches (JSW) 40a-40d are always fixed as shown by solid lines. More particularly, assume now that the slip between the incoming terminal of the junctor switch 40a is 0, the slip of the junctor switch 40b is 1, that of the junctor switch 40c is 2, that of the junctor switch 40d is 3. "Slip 0" means that the numbers of the incoming and outgoing sides of the junctor switch are the same. "Slip 1" means that the outgoing side terminal number is equal to the incoming side terminal number ± 1 of the junctor switch, "slip 2" means that the outgoing side terminal number is equal to the incoming side terminal number ± 2 , and "slip 3" means that the outgoing side terminal 70 number is equal to the incoming side terminal ± 3 . In this embodiment, the incoming and outgoing terminals of the junctor switch are arranged symmetrically for the purpose of effecting so-called pair control, that is for the purpose of controlling both time 75 switches TSW-F and TSW-B by the common holding memory (HM) 32.

The arrangement described above is called a "perfect link configuration" in which the junctor is balanced between one time switch TSW-F and the other 80 time switch TSW-B.

Suppose now that the traffic flow between two time switches TSW-F (#1) and TSW-B (#4) increases so that one junctor highway can not convey all the traffic flow. In this case, the problem of the unbalanced traffic flow can be solved by assigning the 85 traffic flow corresponding to certain channels to the time switches of the junctor switch JSW1, for example carrying larger traffic flow as shown by dotted lines.

The size of the junctor switch matrix is the same as the number of the time switches TSW-F and TSW-B that is the number of the speech path units (SPU), so that such matrix can be fabricated with hardwares easily. If the number of the junctor highway to one 100 time switch is 4, where the maximum number (M) of the speech path unit (SPU) 20 is 16, the total number of the junctor highways is 128 which is one half of the time switches arranged in two stages shown in Fig. 10b pages 60 and 61 of "Communication et Electronique" No. 43, 1973, Oct. "Roseaux de connexion temporels a grande capacite". As will be described later, in Fig. 5 it is also possible to decrease the 105 number of the hardwares of the demultiplexer circuit (DMPX) 43 of the primary time switch (TSW-F) and of the multiplexer circuit (MPX) 41' of the secondary time switch (TSW-B) than the prior art.

Fig. 7 shows a connection where M=8. The permanent connection pattern of the junctor switches JSWa - JSWd is the same as that shown in Fig. 6 and 110 is shown by solid lines. In this connection, the speech path from time switch TSW-F #1 can be established only to time switch TSW-B #1-#4. Thus, it is impossible to establish speech paths to #5-#8 of the time switch TSW-B. Accordingly, in this case, the 115 connection patterns of the junctor switches JSWa - JSWd are changed as shown by dotted lines. Then it becomes possible to establish speech paths also to #5-#8 of the time switch TSW-B. Such change of the connection can be readily done by changing the 120 content of the junctor holding memory circuit (JHM)

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37a which is provided in common for the junctor switches.

Accordingly, it is possible to establish speech paths from time switch TSW-F to all time switches TSW-B by forming the connection pattern of the junctor switch JSW such that one half of the channels of one time division multiplexed frame are connected as shown by solid lines and that the other one half connected, on the time division basis, as shown by dotted lines. In this case too, it is possible to reduce the number of the holding memory devices of the secondary time switches which are controlled in pairs by making symmetrical the connection pattern of the junctor switches JSW. Similar to the case shown in Fig. 6 where $M=4$, an increase of the traffic flow between one time switch TSW-F and a specific time switch TSW-B can be accommodated by partially modifying the connection pattern of the junctor switch so as to increase the capacity of the junctor between specific time switches.

While in the foregoing description, the operation and the feature have been described with regard to cases where $M=4$ and $M=8$, other value of M may be selected. Furthermore, it is to be understood that instead of changing the connection pattern of the junctor time switches JSW in terms of a single channel unit, the change may be made in terms of a bundle unit of several to several tens channels depending upon the value of M , the regulation regarding the probability of internal blocking, the assignment of the highway to time switches, the maximum capacity of the speech path network, etc. In any case, it is possible to decrease the number of holding memory devices to a fraction or only few percent of the number of a case wherein the number of the holding memory device which defines the connection pattern of the junctor switches JSW is varied for each channel.

Change of the connection pattern of the junctor switches is necessary not only when the traffic flow becomes unbalanced but also when it is desired to expand the network, in the same manner as in conventional telephone exchangers.

In this embodiment, the junctor switches are collectively arranged, but they may be dispersed. For example, the hardwares comprising the junctor switches JSW may be distributed among primary or secondary time switches. The principle of operation of such distributed arrangement is the same as that of the collective arrangement.

The construction of the junctor switches JSW is similar to that of a well known space (S) switch except that the change of the connection pattern is not necessary for the processing of ordinary calls, and that the change is made in terms of a bundle of several to several tens channels.

Change of the junctor pattern is necessary when it becomes necessary to transfer to a stand-by speech path unit (SPU) 20x upon occurrence of a failure of a certain speech path unit 20. As above described since the change of the junctor pattern is made in terms of a bundle of several to several tens channels, it is possible to decrease the data writing operations for the junctor holding memory device (JHM) 37a to a fraction, thus enabling rapid remedy of the fault.

The redundant switching performance of the speech path unit SPU, that is the operation of the incoming transfer switch TRF and the outgoing transfer switch TRB will be described hereunder with reference to Fig. 8. More particularly, the incoming transfer switch TRF comprises two transfer switches U and V with the stationary contacts thereof on the opposite sides (upper and low sides) connected together. To the stationary contacts au and bv is connected an input highway 23a from the synchronizing circuit SYNC or the CODEC, whereas a maintenance outgoing highway 24a from test unit (TSTU) 21 is connected to the stationary contacts bu and av. The movable contact cu of the transfer switch U is connected to the forward time division speech path connecting equipment TDC-F of a speech path unit through a highway 23a, whereas the movable contact cv of the transfer switch V is connected to the incoming transfer switch TRF of the next stage or to a stand-by or spare mode speech path unit 20x.

Similarly, the outgoing transfer switch TRB comprises two transfer switches W and X with their stationary contacts on the opposite sides connected together. The stationary contacts bw and ax are connected to the test unit (TSTU) 21 via the maintenance incoming highway 24b, while the stationary contacts aw and bx are connected to an outgoing highway 23b leading to the synchronizing circuit SYNC or the CODEC. The movable contact cw of the transfer switch W is connected to the highway 23b from the backward time division speech path connecting equipment TDC-B of a speech path unit SPU, whereas the movable contact cx of the transfer switch X is connected to the highway 24b from another outgoing transfer switch TRB or a stand-by speech path unit SPU 20x. These incoming and outgoing transfer switches TRF and TRB are paired for respective speech path units (SPU), and the paired transfer switches U, V, W and X are transferred by a signal from the central processing unit (CPU) 28 via maintenance signal distributor (MSD) 28a. These transfer switches may be mechanical or electric switches.

The operations of the incoming and outgoing transfer switches TRF and TRB will be described hereunder with reference to Figs. 2, 9A and 9B.

Assume now that all transfer switches TRF and TRB shown in Fig. 2 are thrown to the side "a" and that all speech path units #1-#a are operating normally. Under these conditions, the incoming transfer switch TRF establishes a path which interconnects the input highway 23a and the onward time division speech path connecting equipment TDC-F of the speech path unit and a path which interconnects the test unit (TSTU) 21 and a stand-by speech path unit 20x. The outgoing transfer switch TRB establishes a path which interconnects the backward time division speech path connecting equipment TDC-B of the speech path unit and the outgoing highway 23b and a path interconnecting the stand-by speech path unit 20x and the test unit (TSTU) 21. Consequently, the incoming and outgoing highways, the CODEC and the synchronizing circuit SYNC, not shown, the forward and backward time division speech path con-

- necting equipments TDC-F, TDC-B, the test unit (TSTU) 21 and the stand-by speech path unit 20x are interconnected. These states are diagrammatically represented by Fig. 9A. Accordingly, in this case, the 5 test unit 21 performs the validity check of the stand-by speech path unit 20x. In Fig. 9, shaded blocks represent elements under test.

When a fault occurs on a #1 speech path unit 20a, for example, so that the transfer switches (TRF) 22a 10 and (TRB) 25a on their incoming and outgoing sides are thrown to contact "b", the TDC-F and TDC-B of #1 speech path unit 20a are connected to the test unit (TSTU) 21 whereas the incoming and outgoing highways 23a and 23b are connected to the #x 15 stand-by speech path unit 20x through maintainance highways 24a and 24b. Thus, the test unit 21 tests the faulty #1 speech path unit 20a to locate the faulty point by checking the received and transmitted signals or by using other measures, and informs the test 20 result to the central processing unit.

Fig. 10 shows a modified embodiment of the digital telephone switching system of this invention which is constructed to promptly detect a faulty equipment, and to execute processing of the transfer 25 to the stand-by equipment thereby continuing the switching operation. The embodiment shown in Fig. 10 comprises a supervisory equipment (SV) 50 and supervisory information lines (SL) 51 which inter-connect the supervisory equipment 50 and respective speech path units 20a-20n and 20x. When such 30 important and common fault as, for example, the fault of the power circuit, a fault of the clock signal source and a fault of the control information distributing circuit occurs in the speech path unit or the 35 junctor switch units (JSU) 26a and 26b, a signal representing such fault is sent to the supervisory equipment 50 through the supervisory lines 51. The number of the supervisory lines (SL) 51 which inter-connect the speech path units and the supervisory 40 equipment is made a minimum. The supervisory equipment 50 promptly informs the fault to the central processing unit 28 according to the content of the supervisory lines 51. As an expedient of informing the fault from the supervisory equipment 50 to 45 the central processing unit 28 may be used a periodical looking-in operation by the central processing unit 28 or a forced interruption by the supervisory equipment 50. Which one of the expedients is to be used is determined by considering the required service 50 grade, service quality, etc.

The operation of the junctor switch unit JSU will be described hereunder with reference to Fig. 11. It should be remembered that the performance of the junctor switch unit JSU is to control the junctor performance between the time switches TSW in a plurality of speech path units (SPU). Thus, the junctor switch unit is operated when the network is to be expanded due to the addition of the speech path units, or when a fault occurs on a speech path unit or 55 when transfer connecting the incoming and outgoing highways 23a and 23b of a specific speech path unit SPU to the #x stand-by speech path unit 20x. The junctor switch unit JSUa is constituted by a plurality of time division junctor switches (JSW) 60 (only JSWa is shown) and a junctor switch holding 65 memory circuit (JHM) 37a which commonly controls the plurality of time division junctor switches (JSW).

The system shown in Fig. 11 is duplicated by providing two systems 26a and 26x of the junctor switch unit JSU constructed as above described.

The transfer operations of the junctor switch unit when a fault occurs are as follows. Assume now 70 consider a transfer operation by which a signal on the #1 highway 23a of the #1 speech path unit 20a is transferred to the #1 highway 23b and the #n highway 23b of speech path units 20a and 20n is transferred, as shown by solid lines. Due to the fault of the speech path unit 20a when the #x stand-by speech path unit 20x is used to perform the switching operation, under the control of the central processing unit, the status of the transfer switches TRF, TRB and of the junctor holding memory circuit (JHM) 37a of the time division junctor switch JSWa are changed. Such status changes are made, under the control of 80 the control unit (CPU), to transfer the #1 transfer switches TRF and TRB to the #n speech path unit 20x for setting the status of the time switch TSW and the digital trunk circuit DTRK in the #x speech path unit 20x similar to the status in the #1 speech path 85 unit 20a thereby transferring the content of the junctor holding memory circuit (JHM) 37a to the #x speech path unit 20x from the #1 speech path unit 20a. Consequently, it is possible to assure normal transfer operation even when #1 speech path unit 90 (SPU) 20a becomes faulty. When the #1 TRF, JHM 37x, #1 TRJ and #1 TRB are set as shown in Fig. 11 so as to pass a test current to the #1 faulty speech path unit 20a through a dot and dash line path shown in Fig. 11 from the test unit 21, it is possible to 95 100 accordingly locate the fault position in the #1 speech path unit 20a and to isolate the faulty speech path unit from the line without interfering the normal switching operation.

The junctor transfer switch TRJ is connected in 105 each speech path unit in front of the time switch TSW-B thereby selecting a junctor switch unit JSU 26a or JSU 26x by the speech path control equipment SPC in each speech path unit SPU. In this manner, since the junctor switch JSWa of JSU 26a or the 110 junctor switch JSWx of JSU 26x is selectively connected to each speech path unit SPU it is possible to independently use the junctor switch JSW for an on-line system and an off-line system thus preventing the fault test from adversely effecting the normal 115 system.

Since the junctor transfer switch TRJ selects either JSU 26a or JSU 26x of each speech path unit, even when the junctor transfer switch TRJ of a specific speech path unit becomes faulty, the fault would be 120 limited to only the specific speech path unit whereby there is no adverse effect upon the entire transfer system. If the junctor transfer switches TRJ were collectively installed in an junctor switch unit, for example, the fault in that TRJ would affect the entire 125 transfer system which is of course objectional.

Fig. 12 shows still further modification of this invention which is especially suitable for a situation where the incoming and outgoing lines of a time division telephone switching system are not limited 130 to time division multiplexed highways but include

lines for transmitting voice signals and inter-office connection signals without varying them. The system comprises a trunk circuit 55, a CODEC 56, and a voice signal line (VL) 57. The voice signal comprises 5 a signal exchanged between telephone exchange offices, and an analogue voice signal before it is converted into a digital multiplexed signal, so that it is impossible to directly connect the voice signal line (VL) 57 to the speech path unit SPU and the central 10 processing unit 28. Accordingly, it is necessary to extract, insert and convert these signals with the trunk circuit (T) 55 and the CODEC (c) 56. The trunk circuit 55 is identical to that utilized in the conventional space division type electric switching system 15 and connected to the central processing unit 28 via line 58 for supervising the status of speech-(busy or idle). In addition to the transmission and reception of the dial pulse in the form of interrupted or inverted direct current, the trunk circuit performs a portion of 20 the processing of various signals which have been performed by the central processing unit 28. The purpose of CODEC 56 is to convert analogue voice signals into digital multiplexed signals with the same multiplicity and the same signal speed as the 25 incoming and outgoing highways 23a and 23b of each speech path unit. The multi-frequency signals interchanged between offices are converted into digital signals by CODEC 56 and then transmitted and received through digital trunk circuit DTRK in a 30 given speech path unit.

As above described, by connecting the signal on the voice frequency line 57 to a speech path unit SPU and to the central processing unit 28 it is possible to efficiently process the transfer operation, just like the 35 other embodiments, even where the lines connected to the time division telephone switching system include voice band lines in addition to multiplexed highways.

Fig. 13 shows still further embodiment of this 40 invention in which processors are provided corresponding to respective speech path units 20a-20n, 20x, test unit (TSTU) 21, and junctor switch units (JSU) 26a and 26x so that the processings to the time switches TSW in the speech path units 20a-20n, 20x 45 and to the digital trunk circuit DTRK are independently performed by network processors (NWP) 61a-61n, 61x respectively, and only the processings involving a plurality of networks 60a-60n, 60x, for example, the connection processings between different networks NW, the test processing, and the 50 processing of the junctor connection patterns at the time of expanding the network NW, the communication between other network processors NWP, or junctor switch processors (JPS) 65a, 65x, or system 55 processors SYSP 63 are executed through an inter-processor bus line (IPB) 64, under the supervision of the system processor (SYSP) 63 which contains common data which are referred to if necessary. The test unit (TSTU) 21 is controlled by a test processor 60 TSTP 66 in the same manner as by the speech path unit SPU.

As above described, the network processor (NWP) 61, test processor (TSTP) 66, junctor switch processor (JSP) 65 are distributed among the speech path 65 unit SPU, test unit TSTU, junctor switch unit JSU

which are the objects to be controlled. On the otherhand, the processing of basic exchange is performed by network processor NWP, test processor TSTP, and junctor switch processor JSP. As has 70 been described in connection with the embodiment shown in Fig. 5 it is possible to reduce the amount of communications between respective processors since the entire speech path construction is simple and since of any change of the connection pattern 75 corresponding to a call of a junctor switch is not necessary. By distributing the network processor NWP in the above described manner, even when a plurality of faults generate at the same time, the operation of the entire exchange office would not 80 stop thus assuring high reliability of the communication network.

Although in the descriptions and drawings referred to hereinabove, the highways 23a, 23b, 27a, 27b, 24a, 24b, and voice frequency line (VL) 57 were treated as single lines respectively. In practice, however, they are provided in plural, the number thereof being determined in accordance with the multiplicity of the signals passing through the highways, the operating speed of such component elements as 90 memory devices that constitute the time switches TSW, the maximum desired capacity of the network, and the number of the speech path units.

The detail of the time switch constituting a speech path unit SPU will be described as follows. Where 95 each voice channel comprises 8 bits, for example, and where 8 buffer memory devices which store voice signal are connected in parallel for the purpose of decreasing the operating speed of the memory elements utilized the access speed to each memory 100 element is reduced to 1/8.

Fig. 14 shows the construction of the parallelly connected time switch just described, as shown, the time switch comprises incoming and outgoing highways 70a and 70b respectively multiplexed in K 105 channels, a serial-parallel converter (SPC) 72 which converts the signals on the incoming highway 70a into 8 bit parallel signals, a parallel-serial converter (PSC) 72 which converts the 8 bit parallel signals into signals supplied to the outgoing highway 70b, buffer 110 memory devices 73, 73₈ which store digitalized voice frequency signals arriving over the incoming highway 70a, and a counter (CTR) 75. It is well known that the signal speed on the incoming highway 70a multiplexed into K channels is K x 64 Kb/s in the case of 115 an ordinary 8 bit encoded PCM signals. Thus for example, where the value of K is equal to 128, the speed of the signal on the incoming highway 70a is equal to 8.192 Mb/s. The writing and reading out of the time switch TSW are performed alternately by 120 the counter CTR 75 and the holding memory (HM) 32 so as to perform timed exchange. When this switch is constructed as shown in Fig. 14, as it is possible to decrease the signal speed on the incoming highway 70a to 1/8 by the serial-parallel converter (SPC) 71, the signal speed supplied to the buffer memory 125 devices 73, through 73₈, is decreased to 1.024 Mb/s. Due to the principle of operation of the time switch the sequential writing by the counter (CTR) 75 and the random read out by the holding memory device (HM) 32 are repeated alternately and the operating 130

speed of the buffer memory device BM increase to twice of 1.024 Mb/s.

According to still further modification of this invention a buffer memory device, for example BM, shown in Fig. 14 is divided into a plurality of blocks so as to simultaneously effect the sequential writing or reading out for the plurality of blocks, thus decreasing the necessary speed of the buffer memory device to about one half of the speed described above. If desired, the order of writing and reading out of the buffer memory device may be reversed for effecting the read write operation. In the following description both modes will be described.

Fig. 15 shows one example of such time switch, and the entire system is termed a "time switch module TSM 95". In Fig. 15, elements corresponding to those shown in Fig. 14 are designated by the same reference characters. 80, 80₁, 80₂ . . . 80, show memory blocks M obtained by dividing a buffer memory device, for example BM, shown in Fig. 14. Each block is provided with a data input terminal Di, a data output terminal Do, an address input terminal Add, a write enable terminal WE, and a block selection terminal BS. Reference characters 81, -81, represent latch circuits (LA) connected to the output terminals Do of respective memory blocks 80, through 80₁, 82 represents an AND gate circuit, 83 an inhibit gate circuit, 85 and 86 decoders (DEC), 87 a selector circuit (SEL) and 88-90 OR gate circuits, ATIM is a signal that designates the pulse widths of WE_P and Rp. Usually, this signal is applied at a definite period.

The operation of the system shown in Fig. 15 will now be described with reference to Figs. 16A-16J, wherein Fig. 16A shows the status of an incoming highway 91 connected to a SPC 71 wherein T represents the width of one time slot of this highway and A, B, C, D, and E represent the contents of respective time slots of the incoming highway 91. Fig. 16B represents the content of the counter 75, especially the count of the lower order bit. Fig. 16C show a read/write (R/W) signal produced by decoder 86 in accordance with the output of counter 75 in which R represent a read out cycle while W a writing cycle. Fig. 16D represents the timing of memory access. Fig. 16E represents the sequential addresses SQ represented by the upper order bits of the output of the counter 75 in which P, P+1 in the waveform show an address common to all memory blocks. Fig. 16F shows a write pulse whereas Fig. 16G the processing of the memory blocks M1-M4 and symbols

Add:α(A), Add:β(B) mean that addresses are α and β and their contents are A and B respectively. Further, Fig. 16H shows the waveform of a read out pulse Rp, Fig. 16I shows the waveforms on the outgoing highways 92,-92, of the latch circuits 81,-81, and Fig. 16J represents a random address sent from the holding memory device (HM) 32 in which the symbol, for example, M1-α designates the address α of the memory block (M1) 80₁. As can be noted from Figs. 16A-16J, l=4. Let us assume that the signal sent from the speech path control equipment (SPC) 71 is quadruplexed. In this case the lower order bit corresponding to the output l of the counter 75, that is $\log_2 l$ bits (2 bits, since l=4 in Fig. 16) are decoded by the decoder 86, and one of

the resulting outputs is used as the R/W signal (in Fig. 16, corresponding to a case where the count of lower two bits is 4), and the information (the information D, in the case of Fig. 16A) of a time slot corresponding to the position R where the output of the decoder 86 is "1" is neglected. Then the time slot is assigned to the readout timing (generally speaking a sequential access timing).

The informations on the incoming highway 91 are written in the memory block at a position WE_P shown in Fig. 16F with the write timing W (W side of the waveform R/W) shown in Fig. 16C thus selecting the address of the holding memory device 32 by the selector 87. This is generally called a random address RN and the upper order bits thereof are decoded by decoder 85. In a case where l=4, the output signal of the decoder 85 appears on only one of 4 output terminals. This output signal corresponds to a block select BS of respective memory devices. Accordingly, the R/W signal applied to one input of the OR gate circuits 88-90 is "0" so that only one BS terminal of four memory blocks is designated so as to write data in the designated address above of the memory block. This is shown by an arrow from Fig. 16A to Fig. 16G and the information "A" on the incoming highway 91 is written in address α of the memory block 80₁. As a consequence the content of address α becomes "A" whereas "B" is written into the address β of the memory block (M4) 80₄ (in Fig. 15 l=4) so that the content of address β becomes "B".

One negligible time slot appears, at each 4 time slots as above described, on the information train on the incoming highway 71 which is synchronous with the common clock signal CLK (in Fig. 16B, at a position where the count of the lower 2 bits of the counter 75 is 4). No writing operation is necessary for this negligible time slot (information D shown in Fig. 16A). Since this timing position is decoded by the decoder 86 and used as a read out timing, this time position, that is the count 4 of the lower two bits of the counter 75 is decoded by the decoder 86 to produce a R/W equal (shown in Fig. 16C) on its output. When this R/W signal becomes "1" the selector 87 selects a SQ side address (P shown in Fig. 16E) common to the memory blocks M1-M4 thus rendering one inputs of the OR gate circuits to become "1". Thus, the RS of respective memory block becomes "1" (not caused by the output of the decoder 85). Accordingly, the outputs of all memory blocks become effective, and as shown by an arrow extending from Fig. 16G to Fig. 16I, and outputs of these memory blocks (contents of the addresses P of blocks M1 through M4) are applied to the latch circuits 81,-81, and held therein by the read out pulse Rp shown in Fig. 16H.

By the operation described above it is possible to parallelly read out a plurality of memory blocks with a single read out pulse Rp thus independently applying the read out data to four l/4 multiplexed outgoing highways 92,-92. Moreover, there is an advantage that the access time per one frame length of the memory devices can be decreased to l from conventional length 2l.

As has been pointed out hereinabove, the informa-

tion on the incoming highway is neglected once per times. But this does not present any trouble for the reason as follows.

Fig. 17 is a drawing to supplement the description regarding the neglected time slot in which $l=4$. Time switch module (TSM) 95 has the same construction as that shown in Fig. 15 except that $l=4$, and 96 designates a multiplexing circuit (MPX) connected to the input side of the incoming highway 91. The multiplexer 96 is supplied with the lower two bits of the output of the counter 75 in the TSM 95 via control line 97. The numbers of the input terminals I1-I4 of the multiplexer 96 directly correspond to the content of the control line 97 which selects these inputs. The lines 98₁-98₃ connected to the input terminals I1-I3 are PCM highways having low order of multiplicity K/l (where K=4).

Since no highway of the low order of multiplexity is connected to the input terminal I4 of the multiplexer 96, its output, that is the data train on the incoming highway 91 selects input terminal I1 when the content of the control line 97 is one, whereby the data on the highway 98₁ of the low order of multiplicity appears on the incoming highway 91 whereas when the content on the control line 97 is two the input terminal I2 is selected so that the data on the highway 98₂ of the low order multiplicity appears on the incoming highway. When the content of the control line 97 is three, the data on the highway 98₃ of the low order multiplicity appears on the incoming highway 91, but when the content of the control line is four the input terminal I4 will be selected. Thus the data on the incoming highway 91 has no meaning. Accordingly, any effective data would not be lost even when such data (the time slot on the highway 91) is neglected. The content of the control line 97 comprises lower two bits of the output of the counter 75 in the TSM 95, that is equal to the input information of the decoder 86 in the TSM 95. For this reason, by making the output (in the example shown in Fig. 16, 4) of the decoder 86 to correspond to the number of the input terminal (I4 in the case shown in Fig. 17) which is not connected to a highway of the lower order of multiplexity of the multiplexer 96 it is possible to make the negligible time slot on the incoming highway 91 to correspond to a time slot to be neglected (assigned to a read out timing, more particularly a sequential access timing).

The number of the neglected time slots is K/l per one frame and in order to decrease the number of the neglected time slots, the number of the memory block l is increased. Where a spare access timing is necessary to test speech paths, the number of the neglected time slots is increased.

Although in the embodiment shown in Fig. 15, the read out side is sequentially accessed, if desired the write side can be sequentially accessed. Fig. 18 shows an example of the latter case, particularly a time switch module (TSM) 95'. This modification comprises incoming highways which respectively receive the parallel output from the speech path control equipment (SPC) 71, an outgoing highway 72 which sends an output to PSC 72, and a latch circuit (LA) 103 for holding the outputs of memory blocks 80, through 80_l. R'p represents a read out pulse

which is ceases once per l times just like the write pulse WEp shown in Fig. 16E. WE'p represents a write pulse which is generated per l times like the read out pulse Rp shown in Fig. 16F. Other reference characters have same meanings as those shown in Fig. 15.

Fig. 19 shows a time division switching network of two stage construction utilizing a time switch module TSM shown in Fig. 15 or Fig. 18. In Fig. 19, elements 110, through 110_l, have the same construction as the time switch module 95 shown in Fig. 15. Each of these elements comprises four memory devices M1 through M4, whereas elements 112, through 112_l, have the same construction as the time switch module 95' shown in Fig. 18. Each one of these elements comprises four memory devices M1-M4. The detail of the memory devices are not shown. With this construction, since the number of the junctor highways between the primary and secondary time switches is equal to the number of the memory blocks of the primary and secondary time switches it is possible to construct the junctor between the primary and secondary time switches without adding any new circuit. In Fig. 19, the junctor switch unit JSU shown in Fig. 2 is show by dotted line, so that theoretically, the junctors are provided as shown in Fig. 19.

Fig. 20 shows a further modification of the system shown in Fig. 19 in which the number of the memory blocks M1, M2 is reduced to 1/N of the number of the junctor highways and a demultiplexer (DMPX) 120 which divides one highway into a plurality of highways 121₁-121_N is provided on the outside of the primary time switch 110. The divided highways are multiplexed into a single highway by a multiplexer (MPX) 123 provided on the input side of the secondary time switch.

Fig. 21 shows a modification of the system shown in Fig. 20 in which N groups of latch circuits 130₁₋₁-130_{1-N}, 130₂₋₁-130_{2-N} are provided on the output side of the primary time switch 110. The read out pulse Rp shown in Fig. 15 is divided into N systems by a decoder (DEC) 131 which are connected to respective latch circuits. A multiplexer (MPX) 123 is provided on the input side of the secondary time switch 112. With this construction, the operating phase of the junctor highway is divided into N. However, if the same phase is desired, a double buffer construction may be used, that is latch circuits operating at the same timing may be inserted on the output side of the primary time switch. This construction is advantageous for a switching network utilizing a long junctor cable because the signal speed on the junctor highway increases. Furthermore, as the number of the time switch modules (TSM) 95, 95' increases, the number of the junctor highways also increases so that it becomes possible to connect all time switch modules with the junctors.

Fig. 22 shows still further modification of the system shown in Fig. 20 in which the number of the memory blocks has been increased to j times of the number of the junctors. In this case, each group of j memory blocks (M) of the primary time switch 110 is connected to multiplexers (MPX) 135₁, 135₂ . . . and the multiplexed signals are sent to corresponding or

any demultiplexers (DMPX) 136₁, 136₂... on the input side of the secondary time switch 112. The outputs of the demultiplexers are connected to j memory blocks M1-M_j respectively. This construction reduces the number of the junctor highways.

Fig. 23 shows still further modification of the system shown in Fig. 22 in which j bit parallel-serial converter shift registers 140₁, 140₂... are provided for each group of the memory blocks of the primary 10 time switches 110. In the secondary time switch 112, the outputs of the shift registers 140₁, 140₂... are received by corresponding shift registers 141₁, 141₂... for effecting serial-parallel conversion. The operating period of the latch circuits provided on the 15 sequential access side shown in Fig. 15 is decreased to 1/l of that of the random access side thus providing ample operating speed. Accordingly, when shift registers having parallel input-serial output or series input-parallel output performance are substituted for 20 the latch circuits described above, both the latching function and the parallel-serial conversion or serial-parallel conversion function can be manifested. Consequently, serial-parallel conversion performance can be provided for junctor units (a situation 25 wherein the junctor side is sequentially accessed) or for the transmission line side (a situation wherein the transmission line side is sequentially accessed) without adding any component parts.

Although in the embodiments described above, 30 for the purpose of effecting a pair control of the primary and secondary time switches TSW-F and TSW-B of the speech path unit, a holding memory device was used in common thereto, the pair control is not always necessary. Thus, independent memory 35 devices may be used for respective time switches.

Fig. 24A shows still further modification of the system shown in Fig. 19 in which the time switches have two stage construction. More particularly, on the input highway 91 side and on the outgoing highway 40 102 side, memory devices M, for example speech path memory devices, are randomly accessed by holding memory devices HM 150₁, 150₂, 151₁, 151₂, whereas on the junctor side the memory devices are sequentially accessed by counters 153, and 154. For 45 simplifying the description the numbers of the primary and secondary time switches 110 and 112 and made to be two respectively.

In this manner, where the junctor side is sequentially accessed by counters 153 and 154 the content 50 of the speech path memory device M1 in the primary time switch 110, would be transferred to the speech path memory device M1 of the secondary time switch 112, without any change.

It is also possible to use four speech memory 55 devices M11, M12, M21, M22 by using a speech path memory device in common for the primary and secondary time switches as shown in Fig. 24B. This arrangement can eliminate the counters shown in Fig. 24A so that the number of the speech path 60 memory devices M is reduced to one half.

Fig. 25 is a block diagram showing the detail of the system shown in Fig. 24B. In Fig 25, each one of m incoming highways 91₁-91_m is multiplexed by n. In the same manner each one of m outgoing highways 65 102₁-102_m is also multiplexed by n. Each of m²

memory devices 160₁-160_m (M11-M_m) has a capacity of n/m words (this capacity can be increased or decreased depending upon the quantity of the traffic flow and the internal blocking probability). Each one of the holding memory devices 70 150₁-150_m functions as a control memory device which designates the memory number and its address when time-division multiplexed signals arrive over respective highways 91₁-91_m. Each of the 75 holding memory devices 151₁-151_m acts as a control memory device which designates the number of a read out memory device and the address thereof when a signal is read out from a memory device for the purpose of sending the signal to respective 80 highways 102₁-102_m.

Each holding memory device has a storing capacity of n words each having $\log_2 m + \log_2 -$ where $\log_2 m$

85 m bits designate the number of the memory device n while $\log_2 -$ bits designate the address number in the m memory device. Generally stated, the holding memory device 150₁ controls speech memory devices 160₁-160_m, whereas the holding memory device 151₁ controls speech memory devices 160₁-160_m. This method of control will now be described with reference to Fig. 26. Let us assume now that a line 95 having a time slot α of the incoming highway 91₁ is to be connected to a line having a time slot number β of the outgoing highway 102_m. The speech path memory device that can be used for establishing this connection is a memory device 160₁ and an idle 100 address thereof can be selected by a well known central processing apparatus. Suppose now that an idle address "a" of the memory device 160₁ has been designated. Then m is written in the $\log_2 m$ bits of the address α of the holding memory device 150₁, 105 and a is written in the $\log_2 -$ bits so that, at the time m slot β of the outgoing highway 102_m, signal A stored in the address "a" of the speech path memory 110 device 160₁ would be read out. In this manner, the time slot α of the incoming highway 91₁ and the time slot β of the outgoing highway 102_m are connected together. The connection in the opposite direction (the connection between the time slot β of the highway 91₁ and the time slot α of the highway 102_m) is established in the same manner by using the speech path memory device 160_m. At this time, the operating period of the speech path memory device may be n times per frame for writing and reading respectively, so that the total number of the channels that can be exchanged is $n \times m$.

Fig. 27 shows a pair control system incorporated into the system shown in Fig. 25 or 26. In this case, the holding memory devices 170₁-170_m control 115 commonly incoming highway and outgoing highway using the write addresses and the read out addresses of the informations to respective highways. To mutually connect the same highways the speech path memory device is read out during the fore half of one time slot and the data is written into 120 130

the speech path memory device during the later half. Since the time division exchange operation is similar to that of the system shown in Fig. 26, its description is believed unnecessary.

5 The advantages of respective embodiments are as follows.

(1) According to the time division switching system of the invention, the time division switch digital trunk circuit and the speech path control equipment are grouped or integrated for a certain capacity, the junctor connection between integrated speech path units is made by a junctor switch unit (JSU) with a semipermanent path and as the scale of the network expands, the speech path units are piled up like a building block structure. Accordingly, it is possible to readily expand the telephone network and to readily manufacture the telephone switching system.

(2) When line signals are transmitted and received they are put into idle time slots of the incoming and outgoing highways connected to the switching system by using CODECs or synchronizing circuits and then applied to a digital trunk circuit through junctor switch units and time division switches by way of permanent paths. For this reason, not only the hardware but also the softwares of the speech path control equipment can be manufactured as modules.

(3) According to the embodiment of this invention shown in Fig. 2 through 13, the time division switches TDS, the digital trunk circuit DTRK, the onward and backward time division speech path connecting equipments TDC-F, TDC-B, and the speech path control equipment SPC for these equipments which constitute a time division telephone switching system are constructed as an integral unit, and a common spare unit is prepared for a plurality of units. Consequently, when a normally used unit becomes faulty, this unit can be smoothly switched by a transfer switch and a junctor switch. For this reason, it is possible to decrease the amount of job and the amount of program processing not only at the time of fault processing but also of expanding the network.

(4) Transfer operation of the junctor switches is effected by handling a plurality of channels as one bundle or group and the transfer operation is performed only when a traffic flow unbalance occurs, or when trouble occurs in the speech path unit or when the scale of the network is to be expanded, and not for controlling a call. At a consequence, it is possible to decrease the capacity of the memory device utilized in the junctor switch and the amount of control of the holding memory device, thus simplifying the construction.

(5) Furthermore, as shown in Fig. 13, when a traffic flow control device is added to each integral unit made up of the time division switch, the digital trunk circuit, the onward and backward time division speech path connecting equipment and the speech path control equipment so as to permit the traffic flow control device to process the traffic through the network thereby completing a series of traffic flow controls in each integral unit it becomes possible to prevent shut down of the entire switching office even when a specific integral unit becomes faulty and when another integral unit becomes faulty while

said first mentioned faulty unit is being switched to a stand-by or spare mode unit, thus causing double or triple faults.

(5) When considering the selection of an idle speech channel, since the time switch are provided in two stages it is possible to reduce the number of the switching program steps, such as channel alignment. Moreover, with this two stage construction of the time switch there are advantages that the capacity for treating the unbalance in the traffic flow can be increased, and that the rearrangement of the junctor cables can be simplified at the time of expanding the telephone network. More particularly, junctor switches that permit electrical time division reconnection of the junctors are arranged between primary and secondary time switches. Accordingly, under normal condition a specific connection pattern is established but when the traffic flow becomes unbalance or when the network is to be expanded the connection pattern is changed. This connection can solve problems which occurs when two stage time switches are used to construct the telephone network. When changing the connection pattern of the junctor switches it is not always necessary to make each channel to be controllable but the channel can be switched as channel bundle units. This decreases the bit capacity desired for the junctor switch holding memory device thus not only miniaturizing the system but also simplifying the processing of switching network.

(6) According to the embodiments shown in Figs. 13 through 23, since the memory device which constitute the time switch is divided into a plurality of blocks, the multiplexing and demultiplexing circuits become unnecessary when the memory blocks are parallelly accessed thus decreasing the access time of the memory device to one half. This not only alleviates the conditions of requirement for the cycle time of the memory device but also simplifies peripheral circuits associated with the memory device. Furthermore, when a simple two stage time switch having a simple control algorithm is fabricated it is possible to form junctors between primary and secondary time switches without adding any new circuit.

By increasing or decreasing the number of the memory blocks with a predetermined redundancy it is possible to adjust the number of the junctors between the primary and secondary switches without increasing the operating speed of the memory device.

(7) Furthermore, according to the embodiments, shown in Figs. 24 through 27, the speech path memory device in a time switch is divided into a plurality of blocks which are arranged in a matrix so as to enable the incoming highway to access the memory blocks belonging to the same row and the outgoing highway to access the memory blocks of the same column number. As a consequence, it is possible to increase the capacity of the time switch without redundantly using the memory device and without increasing the operating speed thereof. Thus, according to this invention it becomes possible to fabricate a time division switching network by using large capacity time switch which is constituted by an

inexpensive memory device which is suitable to be fabricated as an integrated circuit. Thus, it is possible to readily increase the capacity of a time division switching network. When it is desired to increase further the capacity of the network, the capacity can be increased by combining time switches or space switches in many stages.

Although the invention has been shown and described in terms of specific embodiment, it will be clear that many changes and modifications will be obvious to one skilled in the art.

CLAIMS

1. A time division telephone switching system in which time division multiplexed signals are exchanged, said system comprising:
 - a plurality of speech path units;
 - a junctor switch unit for interconnecting said plurality of speech path units; and
 - a central processing unit for effecting an overall control of said speech path units;
 each one of said speech path unit comprising time division switches for exchanging signals between predetermined time slots, said signals being time-divisioned and multiplexed to a plurality of time slots, a digital trunk circuit means which processes a channel associated signal containing a register signal identification and a line operating state, and a speech path control equipment receiving and distributing control signals, which includes an interface between said time division switches, said digital trunk circuit and said central processing unit;
2. A time division telephone switching system according to claim 1 which further comprises a spare mode speech path unit provided in common for said plurality of speech path units and switching means for substituting said spare mode speech path unit, under control of said central processing, for a speech path unit which is used normally when a fault occurs thereon.
3. A time division telephone switching system according to claim 1 which further comprises a spare mode junctor switch unit and means controlled by said central processing unit for substituting said spare mode junctor switch unit for said junctor switch unit when a fault occurs thereon.
4. A time division telephone switching system wherein said time division speech path unit comprises two cascade connected time switches, said junctor switch unit is arranged between said time switches.
5. A time division telephone switching system in which time division multiplexed signals are exchanged, said system comprising:
 - incoming and outgoing highways each including a plurality of time slots which receive time division multiplexed signals;
 - a plurality of speech path units;
 - a spare mode speech path unit;
 - a junctor switch unit for interconnecting said plurality of speech path units and said spare mode speech path unit;
- 65 speech path unit;

test means;

a time division speech path unit including a pair of change-over switches for switching the connections between respective speech path units, said spare mode speech path unit said incoming and outgoing highways and said test means; and

a central processing unit for providing an overall control of said speech path units and said change-over switches;

- 70 each one of said speech path units including time division switches for exchanging said multiplexed signals between predetermined time slots, a digital trunk circuit which processes a channel associated signal containing a register signal identification and a line operating state, and a speech path control equipment receiving and distributing control signals, which includes an interface between said time division switches, said digital trunk circuit and said central processing unit;
- 75 said junctor switch unit being constructed to establish and reestablish connections between respective speech path units by treating a plurality of time slots as a group, and
- 80 said change-over switch being controlled by said central processing unit for substituting said spare mode speech path unit and said incoming and outgoing highways for a speech path unit which is used normally and a fault occurs therein and for connecting said test means to said faulty speech path unit.
- 85 6. A time division telephone switching system according to claim 5 wherein said test means is normally connected to said spare mode speech path unit through said change-over switch when normally used speech path unit operates normally thereby confirming the normality thereof.
- 90 7. A time division telephone switching system according to claim 5 which further comprises means for constantly supervizing faulty condition of said speech path units and upon occurrence of a fault, said central processing unit controls said change-over switch in response to the output of said supervisory means.
- 95 8. A time division telephone switching system in which time division multiplexed signals are exchanged, said system comprising:
 - a plurality of speech path units;
 - a junctor switch unit for establishing connections between said plurality of speech path units; and
 - a central processing unit for providing overall control of said speech path units;
- 100 each one of said speech path units including time division switches for exchanging said time division multiplexed signals between predetermined time slots, a digital trunk circuit means for processing a channel associated signal containing a register identification and a line operating state, and a speech path control equipment receiving and distributing control signals, which includes an interface between said time division switches, said digital trunk circuit and said central processing unit;
- 105 said junctor switch unit being constructed to establish connections and reconnections between respective speech path units by treating a plurality of time slots as a group; and
- 110 said junctor switch unit including a time division

junctor switch and a junctor switch holding memory device which controls said time division junctor switch under a control of said central processing unit.

5 9. A time division telephone switching system according to claim 8 wherein said junctor switch unit is provided in duplicate.

10. A time division telephone switching system according to claim 8 wherein each one of said

10 speech path units comprises junctor change-over switch means which determines which one of the outputs of it the junctor units of the system should be received, said junctor change-over switch means being under control of said speech path control

15 equipment.

11. A time division telephone exchange system in which time division multiplexed signals are exchanged, said system comprising:

20 a plurality of speech path units;

20 a junctor switch unit for interconnecting said plurality of speech path units;

25 a central processing unit for effecting an overall control of said speech path units;

30 each one of said speech path units including a time division switches for exchanging said signals between predetermined time slots, a digital trunk circuit means for processing a channel associated signal containing a register signal identification and a line operating state, and a speech path control

35 equipment receiving and distributing control signals which includes an interface between said time division switches, said digital trunk circuit and said central processing unit;

40 said junctor switch unit being constructed to establish and reestablish connections between respective speech path units by treating a plurality of time slots as a group;

45 an additional trunk circuit means which supervizes a speech state of an analogue line, transmits and receives a dial pulse and shares a portion of the processings of various signals executed by said central processing unit; and

50 means connected to the output of said additional trunk circuit means for converting a voice signal into a form that can be applied to and taken out from said time division switches.

55 12. A time division telephone switching system in which a time division multiplexed signals are exchanged, said system comprising:

50 a plurality of speech path units;

55 a junctor switch unit for interconnecting said plurality of speech channel units;

60 a central processing unit for providing an overall control of said speech path units;

65 each one of said speech path units including a time division switches for exchanging said signals between predetermined time slots, a digital trunk circuit means for processing a channel associated signal containing a register signal identification and a line operating state, and a speech path control

70 equipment receiving and distributing a control signal, which includes an interface between said time division switches, said digital trunk circuit means and said central processing unit;

75 said junctor switch unit being constructed to

70 establish connections and reconnections between said speech channel units by treating a plurality of time slots as a group;

75 control means for processing in each speech path unit and in each junctor switch unit; and

80 said central processing unit executing only processes involving a plurality of speech path units and supervising the operation of the control means in each speech path unit.

80 13. A time division telephone switching system in which a time division multiplexed signals are exchanged, said system comprising:

85 a plurality of speech path units;

85 a junctor switch unit for interconnecting said plurality of speech path units; and

90 a central processing unit for effecting an overall control of said speech path units;

95 each one of said speech channel units including a time division switches for exchanging signals between predetermined time slots, a digital trunk circuit means for processing a channel associated signal containing a register signal identification and a line operating state, and a speech path control equipment receiving and distributing control signals,

100 which includes an interface between said time division switches, said digital trunk circuit means, and said central processing unit;

105 said junctor switch unit being constructed to establish connections and reconnections between said speech path units by treating a plurality of time slots as a group;

105 said time division switches including memory means for temporarily storing a speech information at the time of a switching operation, said memory

110 means being divided into a plurality of memory blocks;

110 means for accessing a predetermined one of said memory blocks at an access time on a random access side of said memory means; and

115 means for parallel accessing a plurality of memory blocks at an access time on a sequential access side of said memory means, thereby writing and reading said speech information, wherein K/l of the multiplicity of the highway on the random access side are used as invalid time slots, and a random access time corresponding to said invalid time slot is also used as a sequential access time where K represents the multiplicity of a highway on the random access side and l represents the number of said blocks of said memory means.

120 14. A time division telephone switching system according to claim 13 which further comprises a shift register which operates as a serial input and parallel output type on said sequential access side.

125 15. A time division telephone switching system according to claim 13 wherein the number of blocks of said memory means is variable.

125 16. A time division telephone switching system according to claim 13 wherein a portion of said invalid time slot is operated at a spare access time.

130 17. A time division telephone switching system in which time division multiplexed signals are exchanged, said system comprising:

130 a plurality of speech path units;

130 a junctor switch unit for interconnecting said plur-

ality of speech path units; and a central processing unit for effecting an overall control of said speech path units; each one of said speech channel units including a

5 time division switches for exchanging signals between predetermined time slots, a digital trunk circuit means for processing a channel associated signal containing a register signal identification and a line operating state, and a speech path control equipment receiving and distributing control signals, which includes an interface between said time division switches, said digital trunk circuit means and said central processing unit; said junctor switch unit being constructed to

15 establish connections and reconnections between said speech path units by treating a plurality of time slots as a group; said time division switches being constructed in two stages and including memory means for temporarily storing a speech information at the time of switching, said memory means being divided into a plurality of memory blocks; means for accessing a predetermined one of said memory blocks at an access time by randomly

20 accessing either one of a highway on a transmission line side and a highway on a junctor side; means for parallel accessing a plurality of said memory blocks at an access time by sequentially accessing either one of said highways, wherein the

25 number of said memory blocks corresponds to the number of junctor highways, wherein K/l of the multiplicity of the highway on the random access side are used as invalid time slots, and a random access time corresponding to said invalid time slots are

30 used also as a sequential access time where K represents the multiplicity of the highways on the random access side, and l represents the number of the memory blocks.

18. A time division telephone switching system

35 according to claim 17 wherein the number of said memory blocks is $1/N$, wherein N represents the number of junctor highways, and which further comprises a decoder which distributes a data read out by said sequential access among N junctor highways, and a multiplexing circuit which multiplexes N highways into a single highway on a side on which data writing is made by said sequential access.

19. A time division telephone switching system

40 according to claim 17 wherein the number of said memory block is $1/N$, where N represents the number of junctor highways, and wherein said system further comprises N groups of latch circuit provided on the read out side by the sequential access,

45 means for dividing a read out pulse on said read out side into N pulses for applying the same to said N groups of the latch circuits, and a multiplexing circuit which multiplexes N highways into a single highway on a side on which data writing is made by said

50 sequential access.

20. A time division telephone switching system according to claim 17 wherein the number of said memory blocks is N' , where N' represents the number of junctor highways, and wherein said system further comprises a multiplexing circuit which

55 multiplexes the outputs of N' memory blocks into a single highway on a side on which data is read out by sequential access, and a decoder which distributes data among N' highways on a side on which

60 data is written by sequential access.

21. A time division telephone switching system according to claim 17 which further comprises a shift register which acts as a serial input and parallel output type on said sequential access side.

22. A time division telephone switching system according to claim 17 wherein the number of said divided memory blocks is variable.

23. A time division telephone switching system according to claim 17 wherein a portion of said

65 invalid time slot is used at a spare mode access time.

24. A time division multiplexed telephone switching system in which time division multiplexed signals are exchanged said system comprising:

70 a plurality of speech path units;

75 a junctor switch unit for interconnecting said plurality of speech path units;

80 a central processing unit for effecting an overall control of said speech path units;

85 each one of said speech channel units including a

90 time division speech channel unit for exchanging signals between a predetermined time slots, a digital trunk circuit means for processing a channel associated signal containing a register signal identification and a line operating state, and a speech path control

95 equipment receiving and distributing control signals, which includes an interface between said time division speech channel unit, said digital trunk circuit means;

100 said junctor switch unit being constructed to establish connections and reconnections between said plurality of speech path units by using a plurality of time slots as a group;

105 said time division speech path unit including a time switch which includes a speech path memory device for temporarily storing a speech information at the time of switching, said memory device being divided into m^2 memory blocks, where m is an integer larger than 2; said divided memory blocks being assigned with column and row numbers of a

110 matrix having m columns and m rows, means for accessing an incoming highway to a predetermined address of a memory block belonging to a column of said matrix corresponding to said incoming highway, and means for accessing an outgoing highway

115 to a predetermined address of a memory block belonging to a column of said matrix corresponding to said outgoing highway.

25. A time division telephone switching system according to claim 24 wherein the number of the

120 words of each memory block is varied by n/m depending upon such conditions as the efficiency of utilization of a highway, and the internal blocking probability of said telephone switching system, where n represents the multiplicity of said highway

125 and m the number of the column or row of said matrix.

26. A time division telephone switching system in which time division multiplexed signals are exchanged, said system comprising:

130 a plurality of speech channel units;

a junctor switch unit for interconnecting said plurality of speech path units; and
a central processing unit for effecting an overall control of said speech path units;

5 each one of said speech path units including a time division switches for exchanging said signals between predetermined time slots, a digital trunk circuit means for processing a channel associated signal containing a register signal identification and

10 a line operating state, and a speech path control equipment receiving and distributing control signals, which includes an interface between said time division speech channel unit, said digital trunk circuit means and said central processing unit;

15 said junctor switch unit being constructed to establish connections and reconnections between said speech path units by treating a plurality of time slots as a group;
said time division speech path unit including a

20 time switch including a speech path memory device adapted to temporarily store a speech information at the time of switching operation, said memory device being divided into m^2 memory blocks (where m is an integer larger than 2) adapted to control write and

25 read out addresses, said memory blocks being assigned with column and row numbers of a matrix having m columns and m rows, means for accessing an incoming highway to a predetermined address of a memory block belonging to a column of said matrix corresponding to said incoming highway, means for accessing an outgoing highway to a predetermined address of a memory block belonging to a column of said matrix corresponding to said outgoing highway, a holding memory device for commonly controlling a memory block of said speech path memory device for controlling a write address and a memory block for controlling a read out address, means for supplying a write address to a memory block belonging to a row of said matrix corresponding to the number of said address controlling memory device, and means for supplying an read out address to a memory block belonging to a column of said matrix corresponding to the number of said address controlling memory device, thereby

30 causing an access time of said speech path memory device which is allocated to read out operation to proceed and access time allocated to write operation, said access times occurring at least twice per one time slot.

35 27. A time division telephone switching system according to claim 26 wherein the number of the words of each memory block is varied by n/m depending upon such conditions as the efficiency of utilization of the highway and the internal blocking

40 probability of the highway wherein n represents the multiplicity of the highway and m the number of columns or rows of a matrix of said memory blocks.

45 28. A time division telephone switching system substantially as described herein with reference to

50 Figs. 2 to 27 of the accompanying drawings.